FEDL66573-01

OKI Semiconductor

This version: May 2001
Previous version: Feb. 2001

MSM66573 Family

NOTICE: MSM66P573/MSM66Q573Y/MSM66Q573LY are supplied as stock lasts.

GENERAL DESCRIPTION

The MSM66573 family of highly functional CMOS 16-bit single chip microcontrollers utilize the nX-8/500S, Oki's proprietary CPU core.

A wide variety of internal multi-functioned timers provide timer functions such as compare out, capture input, event counter, auto reload, and PWM, and can be used for periodic and timed measurements.
And features such as a clock gear function, dual clock function, STOP/HALT mode, programmable pull-up ports in which individual bits can be programmed, and a small, thin package, the MSM66573 family of microprocessors is optimally suited for the system control of small-sized low power devices.
A three channel serial interface and a high-speed bus interface that has separate address and data buses and does not require external address latches are provided as interfaces to external devices.

With a 16-bit CPU core that enables high-speed 16-bit arithmetic computations and a variety of bit processing functions, this general-purpose microcontroller is optimally suited for Digital Audio devices such as a Mini-Disc and an MP3 player.

The flash ROM version (MSM66Q573L) programmable with a single 3 V power supply (2.4 to 3.6 V) and flash ROM version (MSM66Q573) programmable with a single 5 V power supply (4.5 to 5.5 V) are also included in the family.

APPLICATIONS

Digital Audio Control Systems
PC Peripheral Control Systems
Office Electronics Control Systems

ORDERING INFORMATION

Order Code or Product Name	Package	Remark
MSM66573L-xxTB *1	100-pin plastic TQFP (TQFP 100-P-1414-0.50-K)	Low voltage mask ROM version (2.4 to 3.6 V)
MSM66573-xxTB *1		5V mask ROM version (4.5 to 5.5 V)
MSM66Q573L-NTB *2		MSM66573L flash ROM version (2.4 to 3.6 V)
MSM66Q573-NTB *2		MSM66573 flash ROM version (4.5 to 5.5 V)
MSM66573L-xxWA *1	Chip	MSM66573L Chip version (2.4 to 3.6 V)
MSM66573L-xxLA *1	144-pin plastic LFBGA (P-LFBGA144-1111-0.80)	MSM66573L BGA package version (2.4 to 3.6 V)
MSM66Q573L-NLA *2		MSM66Q573L BGA package version (2.4 to 3.6 V)

*1 : The “xx” of “-xx” stands for the code number.
*2 : The “N” of “-N” stands for the flash ROM, blank version.
When OKI programs and ships the flash ROM, the part number is changed from ”–N” to ”–XX” (code number) , for example, MSM66Q573LY-999TB.

FEATURES

Name	MSM66573L	MSM66573
Operating temperature	–30°C to +70°C	
Power supply voltage / maximum operating frequency	V_{DD}=2.4 to 3.6 V / f=14 MHz	V_{DD}=4.5 to 5.5 V / f=30 MHz
Minimum instruction execution time	143 ns at 14 MHz (2.4 to 3.6 V)	67ns at 30 MHz (4.5 to 5.5 V)
	61µs at 32.768 kHz (2.4 to 3.6/4.5 to 5.5 V)	
Internal ROM size (max. external)	64 KB (1 MB)	
Internal RAM size (max. external)	4 KB (1 MB)	
I/O ports	75 I/O pins (with programmable pull-up resistors) 8 input-only pins	
Timers	16-bit free running timer × 1ch	
	Compare out/capture input × 2ch	
	16-bit auto reload timer (event input/timer out) × 1ch	
	8-bit auto reload timer × 1ch	
	8-bit auto reload timer × 3ch (also fumctions as serial communication baud rate generator)	
	8-bit auto reload timer × 1ch (also functions as Watchdog timer)	
	Watch timer (real-time counter) × 1ch	
	8-bit PWM × 4ch (can also be used as 16-bit PWM × 2ch)	
Serial port	UART × 1ch Synchronous × 1ch UART/ Synchronous × 1ch	
A/D converter	10-bit A/D converter × 8ch	
External interrupt	Non-maskable × 1ch Maskable × 6ch	
Interrupt priority	3 levels	
Others	External bus interface (Separate address and data busses)	
	Bus release function	
	Dual clocks function	
	Clock gear function	
Flash ROM version	MSM66Q573L	MSM66Q573

SPECIAL FEATURES

1. High-performance CPU
The family includes the high-performance CPU, powerful bit manipulation instruction set, full symmetrical addressing mode, and ROM WINDOW function, and also provides the best optimized C compiler support.

2. A variety of power saving modes
Attaching a 32.768-kHz crystal produces a real-time clock signal from the internal clock timer. Use of a single clock in place of dual clocks is possible.
The clock gear function allows a 1/2 × or 1/4 × main clock to be selected for the CPU operating clock.
Switching the CPU clock to 32.768-kHz signal, 1/2 × main clock, or 1/4 × main clock, then produces operation in a low power consumption mode.
The family provides a wide range of standby control functions. In addition to the usual STOP mode that stops the oscillator, there are the quick restart STOP mode that shuts down the CPU and peripherals but leaves the oscillator running, and the HALT mode that shuts down the CPU but leaves the peripherals running.

3. MSM66Q573L and MSM66Q573 with flash memory programmable with single power supply
In addition to the regular mask ROM version, the family includes these versions with 64KB of flash memory that can be programmed using a single power supply.
For the MSM66Q573L, an internal booster circuit derives the necessary program voltage from the device's low (2.4 to 3.6 V) power supply, and the program voltage for the MSM66Q573 is provided with a single 5 V power supply (4.5 to 5.5 V).

4. Multifunction, high-precision A/D converter
The family includes a high-precision 10-bit analog-to-digital converter with eight channels and is ideal for such analog control functions as processing audio signals, processing sensor inputs, detecting key switch states, and controlling battery use in portable equipment. Each channel has its own result register readily accessible from the software. In addition to single-channel conversions, there is also a scan function offering automatic conversion from the user's choice of starting channel through to the last channel.

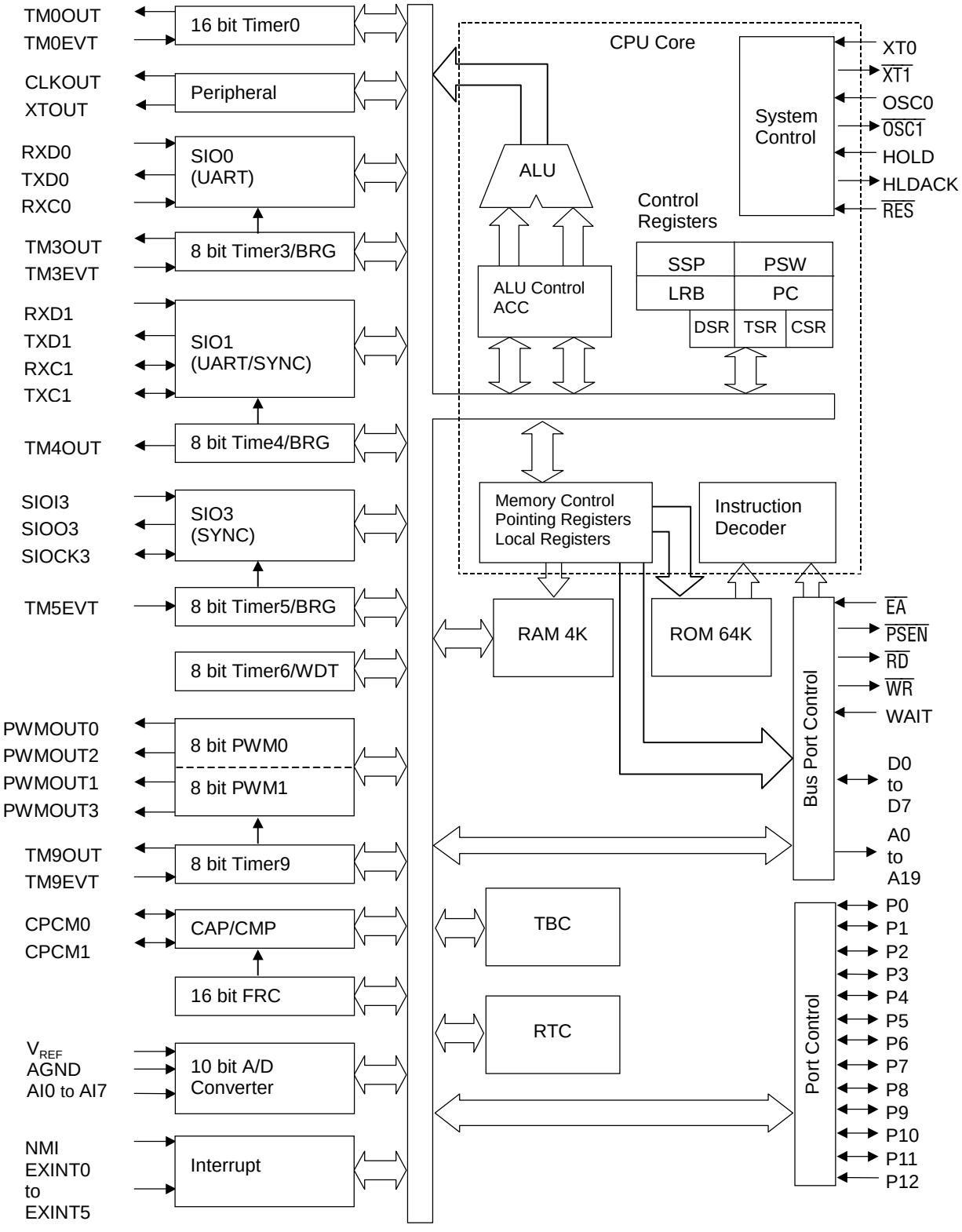
5. Multifunction PWM
The family supports both 8- and 16-bit PWM operation.
Choosing between the time-base counter output or overflow from an 8-bit auto-reload timer as the PWM counter clock source provides a wide number of possibilities over a broad frequency range. The 16-bit PWM configuration supports a high-speed synchronization mode that generates a high-precision output signal with less ripple suitable for digital-to-analog control applications.

6. Programmable pull-up resistors
Building the pull-up resistors into the chip contributes to overall design compactness.
Making them programmable on a per-bit basis allows complete flexibility in circuit board layout and system design. These programmable pull-up resistors are available for all I/O pins not already assigned specific functions (such as the oscillator connection pins).

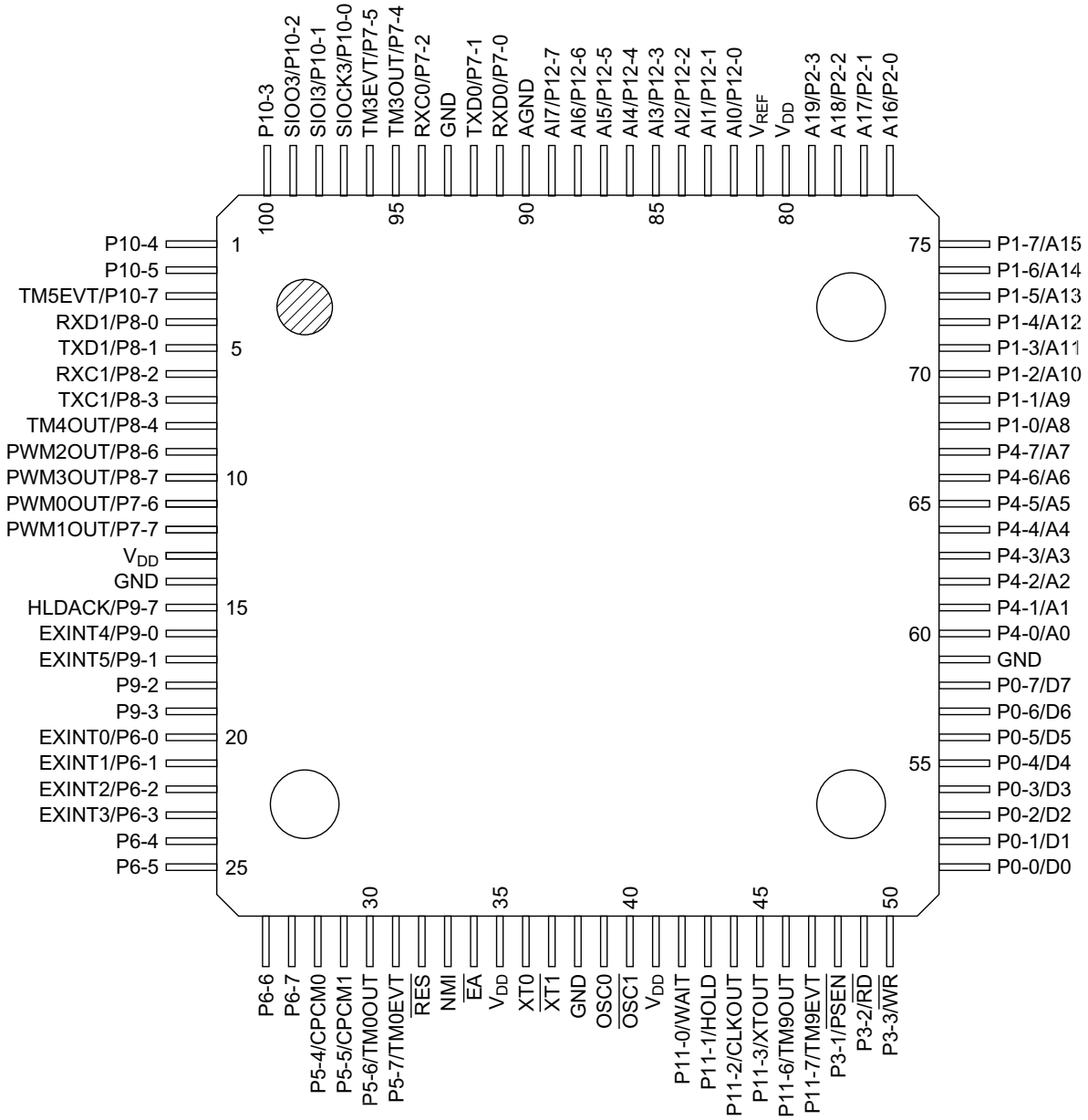
7. High-speed bus interface
The interface to external devices uses separate data and address buses.
This arrangement permits rapid bus access for controlling the system from the microcontroller.

8. Wide support for external interrupts
There are a total of seven interrupt channels for use in communicating with external devices: six for maskable interrupts and one for non-maskable interrupts.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-pin Plastic TQFP

PIN CONFIGURATION (TOP VIEW)

13	12	11	10	9	8	7	6	5	4	3	2	1	
NC	NC	P3-2	P11-7	P11-2	P11-0	NC	XT0	$\overline{EA}$	P5-7	P5-4	P6-6	NC	N
NC	P3-3	P3-1	P11-1	V_{DD}	$\overline{OSC1}$	GND	$\overline{XT1}$	V_{DD}	NMI	P5-6	NC	NC	M
P0-0	P0-2	NC	P11-6	P11-3	OSC0	NC	NC	$\overline{RES}$	P5-5	P6-7	P6-4	P6-5	L
P0-3	P0-5	P0-1	NC	NC	NC	NC	NC	NC	NC	P6-2	P9-3	P6-3	K
P0-6	P0-7	P0-4	NC						NC	P6-1	P9-1	P6-0	J
GND	P4-0	P4-1	NC						NC	P9-7	P9-0	P9-2	H
P4-4	P4-2	P4-3	NC						NC	V_{DD}	P7-7	GND	G
P1-0	P4-6	P4-5	NC						NC	P7-6	P8-7	P8-6	F
P1-2	P4-7	P1-3	NC						NC	P8-1	P8-4	P8-3	E
P1-5	P1-1	P1-4	NC	NC	NC	NC	NC	NC	NC	P10-5	P8-2	P8-0	D
P1-7	P1-6	P2-1	P2-3	P12-0	P12-6	NC	NC	NC	NC	NC	P10-7	P10-4	C
NC	NC	V_{DD}	P12-1	P12-3	P12-5	P12-7	P7-0	P7-1	P7-2	P10-0	P10-2	NC	B
NC	P2-0	P2-2	V_{REF}	P12-2	P12-4	AGND	GND	P7-4	P7-5	P10-1	P10-3	NC	A

144-pin Plastic LFBGA

[Note] Don't connect NC pins with others.

PIN DESCRIPTIONS

In the Type column, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an I/O pin.

Classification	Symbol	Description			
		Type	Primary function	Type	Secondary function
Port	P0_0/D0 to P0_7/D7	I/O	8-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	I/O	External memory access Data I/O port
	P1_0/A8 to P1_7/A15	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P2_0/A16 to P2_3/A19	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P3_1/$\overline{\text{PSEN}}$	I/O	3-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	O	External program memory Access Read strobe output pin
	P3_2/$\overline{\text{RD}}$			O	External data memory access Read strobe output pin
	P3_3/$\overline{\text{WR}}$			O	External data memory access Write strobe output pin
	P4_0/A0 to P4_7/A7	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P5_4/CPCM0	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	Capture 0 input/Compare 0 output pin
	P5_5/CPCM1			I/O	Capture 1 input/Compare 1 output pin
	P5_6/TM0OUT			O	Timer 0 timer output pin
	P5_7/TM0EVT			I	Timer 0 external event input pin
	P6_0/EXINT0	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	I	External interrupt 0 input pin
	P6_1/EXINT1			I	External interrupt 1 input pin
	P6_2/EXINT2			I	External interrupt 2 input pin
	P6_3/EXINT3			I	External interrupt 3 input pin
	P6_4 to P6_7			—	None

Classification	Symbol	Description			
		Type	Primary function	Type	Secondary function
Port	P7_0/RXD0	I/O	7-bit I/O port Pull-up resistors can be specified for each individual bit	I	SIO0 receive data input pin
	P7_1/TXD0			O	SIO0 transmit data output pin
	P7_2/RXC0			I	SIO0 external clock input pin
	P7_4/TM3OUT			O	Timer 3 timer output pin
	P7_5/TM3EVT			I	Timer 3 external event input pin
	P7_6/PWM0OUT			O	PWM0 output pin
	P7_7/PWM1OUT			O	PWM1 output pin
	P8_0/RXD1	I/O	7-bit I/O port Pull-up resistors can be specified for each individual bit	I	SIO1 receive data input pin
	P8_1/TXD1			O	SIO1 transmit data output pin
	P8_2/RXC1			I/O	SIO1 receive clock I/O pin
	P8_3/TXC1			I/O	SIO1 transmit clock I/O pin
	P8_4/TM4OUT			O	Timer 4 timer output pin
	P8_6/PWM2OUT			O	PWM2 output pin
	P8_7/PWM3OUT			O	PWM3 output pin
	P9_0/EXINT4	I/O	5-bit I/O port Pull-up resistors can be specified for each individual bit	I	External Interrupt 4 input pin
	P9_1/EXINT5			I	External Interrupt 5 input pin
	P9_2, P9_3			—	None
	P9_7/HLDACK			O	HOLD mode output pin
	P10_0/SIOCK3	I/O	7-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	SIO3 transmit-receive clock I/O pin
	P10_1/SIOI3			I	SIO3 receive data input pin
	P10_2/SIOO3			O	SIO3 transmit data output pin
	P10_3 to P10_5			—	None
	P10_7/TM5EVT			I	Timer 5 external event input pin
	P11_0/WAIT	I/O	6-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	I	External data memory access wait input pin
	P11_1/HOLD			I	HOLD mode request input pin
	P11_2/CLKOUT			O	Main clock pulse output pin
	P11_3/XTOUT			O	Sub clock pulse output pin
	P11_6/TM9OUT			O	Timer 9 timer output pin
	P11_7/TM9EVT			I	Timer 9 external event input pin
	P12_0/AI0 to P12_7/AI7	I	8-bit input port	I	A/D converter analog input port

Classification	Symbol	Type	Description
Power supply	V_{DD}	I	Power supply pin Connect all V_{DD} pins to the power supply.*
	GND	I	GND pin Connect all GND pins to GND.*
	V_{REF}	I	Analog reference voltage pin (Connect to the V_{DD} pin when A/D converter is not used.)
	AGND	I	Analog GND pin (Connect to the GND pin when A/D converter is not used.)
Oscillation	XT0	I	Sub clock oscillation input pin Connect to a crystal oscillator of f = 32.768 kHz.
	$\overline{XT1}$	O	Sub clock oscillation output pin Connect to a crystal oscillator of f = 32.768 kHz. The clock output is opposite in phase to XT0.
	OSC0	I	Main clock oscillation input pin Connect to a crystal or ceramic oscillator. Or, input an external clock.
	$\overline{OSC1}$	O	Main clock oscillation output pin Connect to a crystal or ceramic oscillator. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.
Reset	$\overline{RES}$	I	Reset input pin
Other	NMI	I	Non-maskable interrupt input pin
	$\overline{EA}$	I	External program memory access input pin If the $\overline{EA}$ pin is enabled (low level), the internal program memory is masked and the CPU executes the program code in external program memory through all address space.

* Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all V_{DD} pins and the ground potential to all GND pins. If a device may have one or more V_{DD} or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Digital power supply voltage	V_{DD}	GND = AGND=0V Ta = 25°C	MSM66573/Q573	–0.3 to +7.0	V
			MSM66Q573Y	–0.3 to +7.0	V
			MSM66573L/Q573L	–0.3 to +4.6	V
			MSM66Q573LY	–0.3 to +4.6	V
Input voltage	V_I		—	–0.3 to V_{DD}+0.3	V
Output voltage	V_O		—	–0.3 to V_{DD}+0.3	V
Analog reference voltage	V_{REF}		—	–0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI}		—	–0.3 to V_{REF}	V
Power dissipation	P_D	Ta = 70°C per package	100-pin TQFP	650	mW
			144-pin LFBGA	750	mW
		Ta = 50°C per package (MSM66Q573LY)	100-pin TQFP	800	mW
			144-pin LFBGA	950	mW
Storage temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Rating	Unit
Digital power supply voltage	V_{DD}	MSM66573/Q573	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	V
		MSM66Q573Y	$f_{OSC} \leq 26$ MHz	4.5 to 5.5	
		MSM66573L/Q573L	$f_{OSC} \leq 14$ MHz	2.4 to 3.6	
		MSM66Q573LY	$f_{OSC} \leq 14$ MHz	2.7 to 3.3	
		MSM66P573	$f_{OSC} \leq 24$ MHz	4.5 to 5.5	
			$f_{OSC} \leq 12$ MHz	2.7 to 3.6	
Analog reference voltage	V_{REF}	—		V_{DD}–0.3 to V_{DD}	
Analog input voltage	V_{AI}	—		AGND to V_{REF}	
Memory hold voltage	V_{DDH}	MSM66573/Q573	f_{OSC}=0Hz	2.0 to 5.5	
		MSM66Q573Y		2.0 to 5.5	
		MSM66573L/Q573L		2.0 to 3.6	
		MSM66Q573LY		2.0 to 3.6	
		MSM66P573		2.0 to 5.5	
Operating frequency	f_{OSC}	MSM66573/Q573	V_{DD}=4.5 to 5.5 V	2 to 30	MHz
		MSM66Q573Y	V_{DD}=4.5 to 5.5 V	2 to 26	
		MSM66573L/Q573L	V_{DD}=2.4 to 3.6 V	2 to 14	
		MSM66Q573LY	V_{DD}=2.7 to 3.3 V	2 to 14	
		MSM66P573	V_{DD}=4.5 to 5.5 V	2 to 24	
			V_{DD}=2.7 to 3.6 V	2 to 12	
	f_{XT}	—		32.768	kHz
Ambient temperature	Ta	Except MSM66Q573LY		–30 to +70	°C
		MSM66Q573LY		–20 to +50	°C
Fan out	N	MOS load		20	—
		TTL load	P0, P3, P11	6	—
			P1, P2, P4, P5, P6, P7, P8, P9, P10	1	—

ALLOWABLE OUTPUT CURRENT VALUES

MSM66573/Q573/Q573Y/P573 (V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)
MSM66573L/Q573L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q573LY (V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)
MSM66P573 (V_{DD} = 2.7 to 3.6V, Ta = –30 to +70°C)

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit
"H" output pin (1 pin)	All output pins	I_{OH}	—	—	–2	mA
"H" output pins (sum total)	Sum total of all output pins	ΣI_{OH}	—	—	–40	
"L" output pin (1 pin)	P0, P3, P11	I_{OL}	—	—	10	
	Other ports				5	
"L" output pins (sum total)	Sum total of P0, P3, P11	ΣI_{OL}	—	—	80	
	Sum total of P1, P2, P4				50	
	Sum total of P5, P6, P9					
	Sum total of P7, P8, P10					
	Sum total of all output pins				140	

[Note]
Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all V_{DD} pins and the ground potential to all GND pins. If a device may have one or more V_{DD} or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

INTERNAL FLASH ROM PROGRAMMING CONDITIONS

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}	MSM66Q573		4.5 to 5.5	V
		MSM66Q573Y		4.5 to 5.5	
		MSM66Q573L		2.4 to 3.6	
		MSM66Q573LY		2.7 to 3.3	
Ambient temperature	Ta	During Read	MSM66Q573	–30 to +70	°C
			MSM66Q573Y	–30 to +70	
			MSM66Q573L	–30 to +70	
			MSM66Q573LY	–20 to +50	
		During Programming		+0 to +50	
Endurance	CEP	—		100	Cycles
Blocks size	—	—		128	bytes

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD} = 4.5 to 5.5 V)

MSM66573/Q573/Q573Y/P573 (V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH}	—		0.44 V_{DD}	—	V_{DD}+0.3	V
"H" input voltage *2, *3, *4, *5, *6				0.80 V_{DD}	—	V_{DD}+0.3	
"L" input voltage *1	V_{IL}	—		–0.3	—	0.16 V_{DD}	
"L" input voltage *2, *3, *4, *5, *6				–0.3	—	0.20 V_{DD}	
"H" output voltage *1, *4	V_{OH}	I_O = –400 µA		V_{DD} – 0.4	—	—	
		I_O = –2.0 mA		V_{DD} – 0.6	—	—	
"H" output voltage *2		I_O = –200 µA		V_{DD} – 0.4	—	—	
		I_O = –2.0 mA		V_{DD} – 0.6	—	—	
"L" output voltage *1, *4	V_{OL}	I_O = 3.2 mA		—	—	0.4	
		I_O = 10.0 mA		—	—	0.8	
"L" output voltage *2		I_O = 1.6 mA		—	—	0.4	
		I_O = 5.0 mA		—	—	0.8	
Input leakage current *3	I_{IH}/I_{IL}	V_I = V_{DD}/0 V		—	—	1/–1	µA
Input current *5				—	—	1/–250	
Input current *6				—	—	15/–15	
output leakage current *1, *2, *4	I_{LO}	V_O = V_{DD}/0 V		—	—	±10	µA
Pull-up resistance	R_{pull}	V_I = 0 V	Except MSM66Q573Y	25	50	100	kΩ
			MSM66Q573Y	15	30	100	kΩ
Input capacitance	C_I	f_{OSC} = 1 MHz, Ta = 25°C		—	5	—	pF
Output capacitance	C_O			—	7	—	
Analog reference supply current	I_{REF}	During A/D operation		—	—	4	mA
		When A/D is stopped		—	—	10	µA

*1: Applicable to P0
*2: Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10
*3: Applicable to P12, $\overline{EA}$, NMI
*4: Applicable to P3, P11
*5: Applicable to $\overline{RES}$
*6: Applicable to OSC0

Supply current (V_{DD} = 4.5 to 5.5 V)

• MSM66573

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode *1	I_{DD}	f_{OSC} = 30 MHz		—	36	55	mA
		f_{XT} = 32.768 kHz		—	60	160	µA
HALT mode *2	I_{DDH}	f_{OSC} = 30 MHz		—	23	35	mA
STOP mode *3	I_{DDS}	OSC is stopped	XT is used	—	5	110	µA
			XT is not used	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C		—	0.2	10	

• MSM66Q573

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode *1	I_{DD}	f_{OSC} = 30 MHz		—	42	70	mA
		f_{XT} = 32.768 kHz		—	500	800	µA
HALT mode *2	I_{DDH}	f_{OSC} = 30 MHz		—	24	40	mA
STOP mode *3	I_{DDS}	OSC is stopped	XT is used	—	5	110	µA
			XT is not used	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C		—	0.2	10	

• MSM66Q573Y

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode *1	I_{DD}	f_{OSC} = 26 MHz		—	42	70	mA
		f_{XT} = 32.768 kHz		—	500	800	µA
HALT mode *2	I_{DDH}	f_{OSC} = 26 MHz		—	24	40	mA
STOP mode *3	I_{DDS}	OSC is stopped	XT is used	—	5	110	µA
			XT is not used	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C		—	0.2	10	

• MSM66P573

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode *1	I_{DD}	f_{OSC} = 24 MHz		—	60	80	mA
		f_{XT} = 32.768 kHz		—	114	300	µA
HALT mode *2	I_{DDH}	f_{OSC} = 24 MHz		—	30	40	mA
STOP mode *3	I_{DDS}	OSC is stopped	XT is used	—	6	120	µA
			XT is not used	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C		—	0.2	10	

[Note] Ports used as inputs are at V_{DD} or 0 V. Other ports are unloaded.
*1. CPU and all the peripheral functions (timer, PWM, A/D, etc.) are activated.
*2. CPU is stopped, and all the peripheral functions (timer, PWM, A/D, etc.) are activated.
*3. CPU and all the peripheral functions are deactivated (The clock timer is being activated when the XT is used).

DC Characteristics 2 (V_{DD} = 2.4 to 3.6 V)

MSM66573L/Q573L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q573LY (V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)
MSM66P573 (V_{DD} = 2.7 to 3.6 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH}	—	0.55V_{DD}	—	V_{DD}+0.3	V
"H" input voltage *2, *3, *4, *5, *6			0.80V_{DD}	—	V_{DD}+0.3	
"L" input voltage *1	V_{IL}	—	–0.3	—	0.16 V_{DD}	
"L" input voltage *2, *3, *4, *5, *6			–0.3	—	0.20 V_{DD}	
"H" output voltage *1, *4	V_{OH}	I_O = –400 µA	V_{DD} – 0.4	—	—	
		I_O = –2.0 mA	V_{DD} – 0.8	—	—	
"H" output voltage *2		I_O = –200 µA	V_{DD} – 0.4	—	—	
		I_O = –1.0 mA	V_{DD} – 0.8	—	—	
"L" output voltage *1, *4	V_{OL}	I_O = 3.2 mA	—	—	0.5	
		I_O = 5.0 mA	—	—	0.9	
"L" output voltage *2		I_O = 1.6 mA	—	—	0.5	
		I_O = 2.5 mA	—	—	0.9	
Input leakage current *3	I_{IH}/I_{IL}	V_I = V_{DD}/0 V	—	—	1/–1	µA
Input current *5			—	—	1/–250	
Input current *6			—	—	15/–15	
output leakage current *1, *2, *4	I_{LO}	V_O = V_{DD}/0 V	—	—	±10	µA
Pull-up resistance	R_{pull}	V_I= 0 V, Except MSM66Q573LY	40	100	200	kΩ
		V_I= 0 V, MSM66Q573LY	20	50	200	
Input capacitance	C_I	f_{OSC} = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance	C_O		—	7	—	
Analog reference supply current	I_{REF}	During A/D operation	—	—	2	mA
		When A/D is stopped	—	—	5	µA

*1: Applicable to P0
*2: Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10
*3: Applicable to P12, $\overline{EA}$, NMI
*4: Applicable to P3, P11
*5: Applicable to $\overline{RES}$
*6: Applicable to OSC0

Supply current (V_{DD} = 2.4 to 3.6 V)

• MSM66573L

(V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode	I_{DD}	f_{OSC} = 14 MHz		—	12	20	mA
		f_{XT} = 32.768 kHz		—	30	130	µA
HALT mode	I_{DDH}	f_{OSC} = 14 MHz		—	7	11	mA
STOP mode	I_{DDS}	OSC is stopped	XT is used*	—	2	110	µA
			XT is not used*	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C*		—	0.2	10	

• MSM66Q573L

(V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode	I_{DD}	f_{OSC} = 14 MHz		—	13	22	MA
		f_{XT} = 32.768 kHz		—	300	600	µA
HALT mode	I_{DDH}	f_{OSC} = 14 MHz		—	7	11	MA
STOP mode	I_{DDS}	OSC is stopped	XT is used*	—	3	110	µA
			XT is not used*	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C*		—	0.2	10	

• MSM66Q573LY

(V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode	I_{DD}	f_{OSC} = 14 MHz		—	15	22	MA
		f_{XT} = 32.768 kHz		—	300	600	µA
HALT mode	I_{DDH}	f_{OSC} = 14 MHz		—	7	11	MA
STOP mode	I_{DDS}	OSC is stopped	XT is used*	—	3	110	µA
			XT is not used*	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C*		—	0.2	10	

• MSM66P573

(V_{DD} = 2.7 to 3.6 V, Ta = –30 to +70°C)

Mode	Symbol	Condition		Min.	Typ.	Max.	Unit
CPU operation mode	I_{DD}	f_{OSC} = 12 MHz		—	17	24	mA
		f_{XT} = 32.768 kHz		—	65	160	µA
HALT mode	I_{DDH}	f_{OSC} = 12 MHz		—	8	12	mA
STOP mode	I_{DDS}	OSC is stopped	XT is used*	—	3	110	µA
			XT is not used*	—	1	100	
		OSC is stopped, XT is not used V_{DD} = 2 V, Ta = 25°C*		—	0.2	10	

[Note] Ports used as inputs are at V_{DD} or 0 V. Other ports are unloaded.
*1. CPU and all the peripheral functions (timer, PWM, A/D, etc.) are activated.
*2. CPU is stopped, and all the peripheral functions (timer, PWM, A/D, etc.) are activated.
*3. CPU and all the peripheral functions are deactivated (The clock timer is being activated when the XT is used).

AC Characteristics 1 (V_{DD} = 4.5 to 5.5 V)

(1) External program memory control

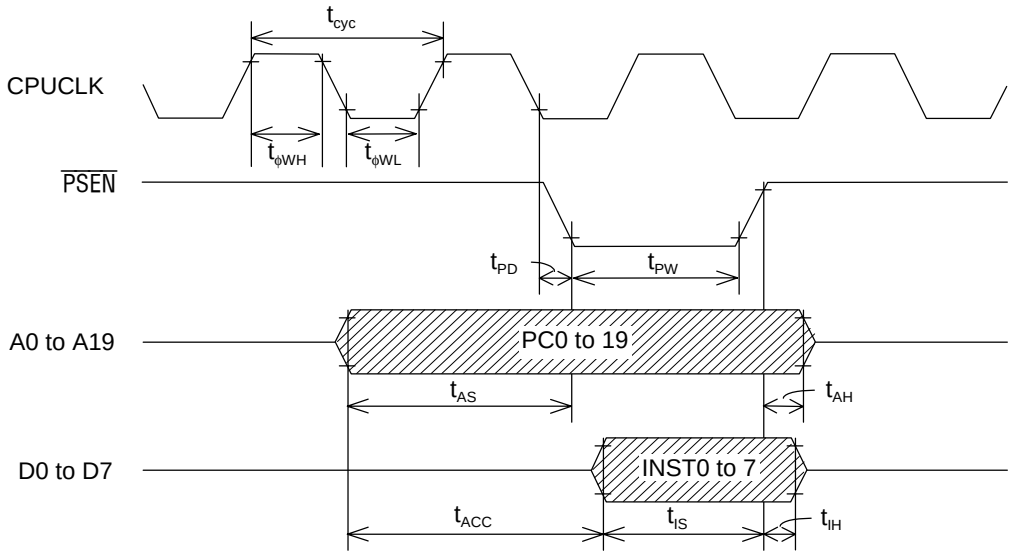
MSM66573/Q573/Q573Y/P573 (V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30/26 MHz	33.3/38.5	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{PSEN}$ pulse width	t_{PW}		2tϕ – 15	—	
$\overline{PSEN}$ pulse delay time	t_{PD}		—	45	
Address setup time	t_{AS}		tϕ – 25	—	
Address hold time	t_{AH}		0	—	
Instruction setup time	t_{IS}		25*1	—	
Instruction hold time	t_{IH}		0	—	
Read data access time	t_{ACC}		—	3tϕ – 65*2	

Note: $t\phi = t_{cyc}/2$

*1: MSM66P573 = 30

*2: MSM66P573 = 3tϕ – 70



Bus timing during no wait cycle time

(2) External data memory control

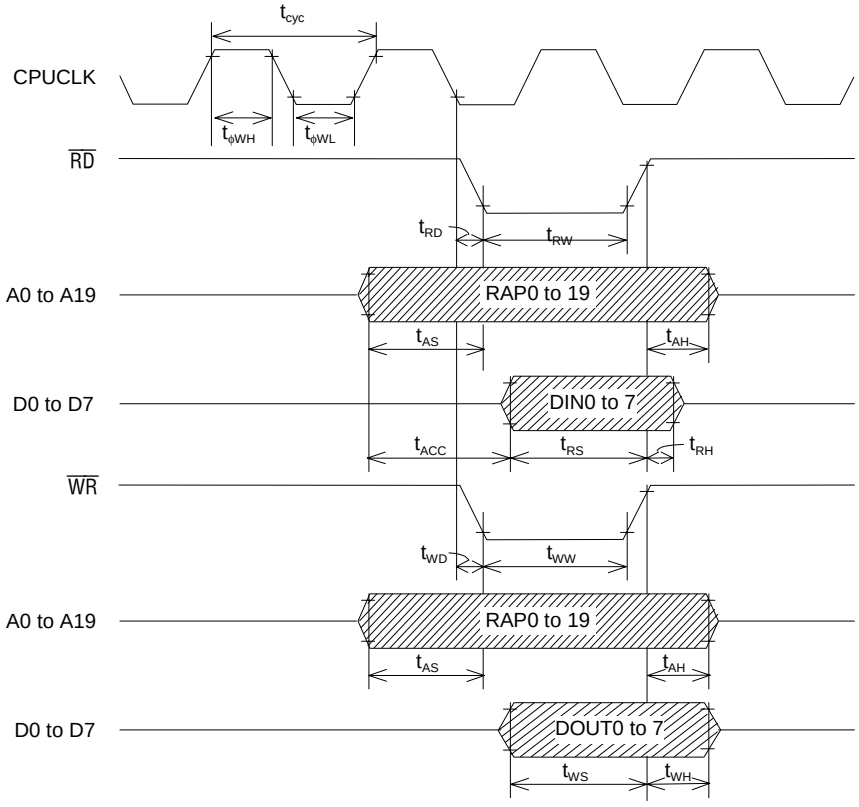
MSM66573/Q573/Q573Y/P573 (V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30/26 MHz	33.3/38.5	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{RD}$ pulse width	t_{RW}		2tϕ – 15	—	
$\overline{WR}$ pulse width	t_{WW}		2tϕ – 15	—	
$\overline{RD}$ pulse delay time	t_{RD}		—	45	
$\overline{WR}$ pulse delay time	t_{WD}		—	45	
Address setup time	t_{AS}		tϕ – 25	—	
Address hold time	t_{AH}		tϕ – 3	—	
Read data setup time	t_{RS}		25*1	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	3tϕ – 65*2	
Write data setup time	t_{WS}		2tϕ – 30	—	
Write data hold time	t_{WH}		tϕ – 3	—	

Note: tϕ = t_{cyc}/2

*1: MSM66P573 = 30

*2: MSM66P573 = 3tϕ – 70



Bus timing during no wait cycle time

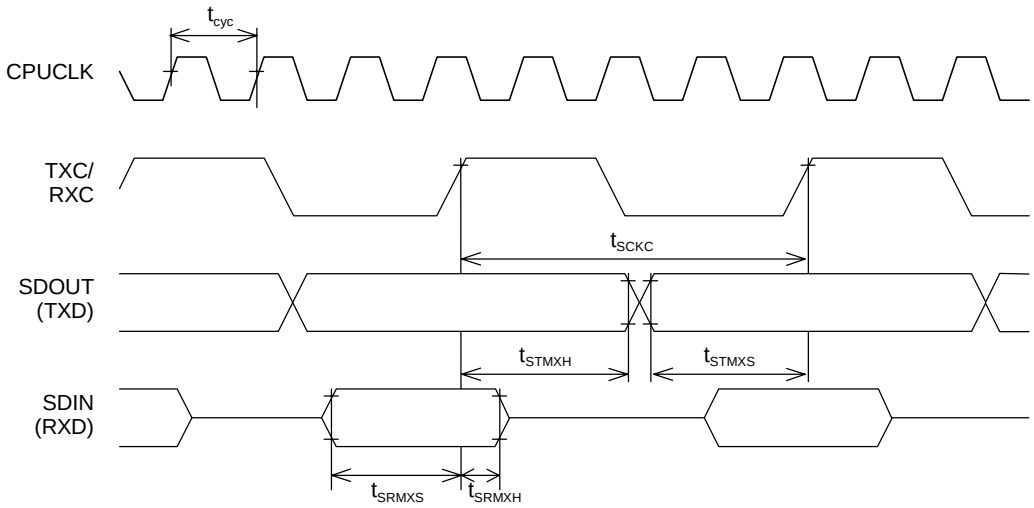
(3) Serial port control

Master mode

MSM66573/Q573/Q573Y/P573 (V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30/26 MHz	33.3/38.5	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	$4t_{cyc}$	—	
Output data setup time	t_{STMXS}		$2t\phi - 5$	—	
Output data hold time	t_{STMXH}		$5t\phi - 10$	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		0	—	

Note: $t\phi = t_{cyc}/2$

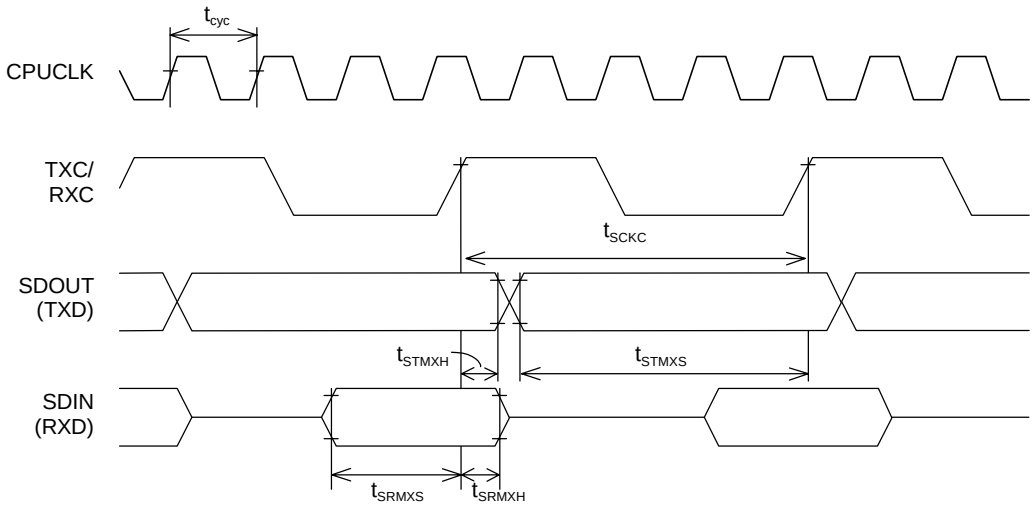


Slave mode

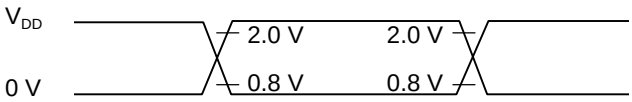
MSM66573/Q573/Q573Y/P573 (V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30/26 MHz	33.3/38.5	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	$4t_{cyc}$	—	
Output data setup time	t_{STMXS}		$2t\phi$ – 15	—	
Output data hold time	t_{STMXH}		$4t\phi$ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		3	—	

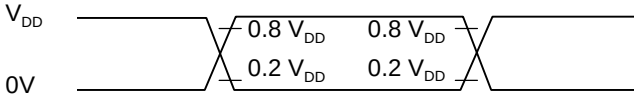
Note: $t\phi = t_{cyc}/2$



Measurement points for AC timing (except the serial port)



Measurement points for AC timing (the serial port)



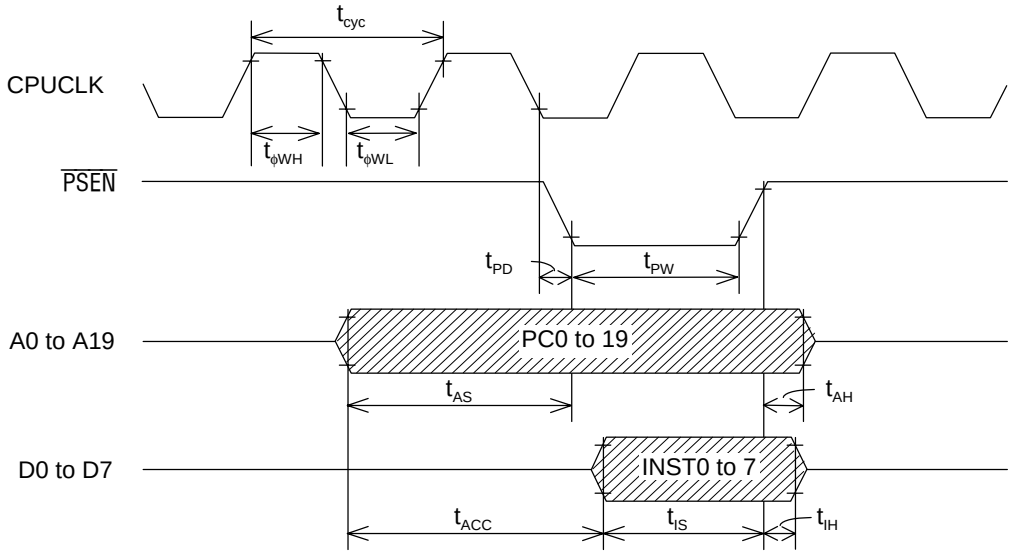
AC Characteristics 2 (V_{DD} = 2.4 to 3.6 V)

(1) External program memory control

MSM66573L/Q573L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q573LY (V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)
MSM66P573 (V_{DD} = 2.7 to 3.6 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{PSEN}$ pulse width	t_{PW}		$2t\phi - 25$*1	—	
$\overline{PSEN}$ pulse delay time	t_{PD}		—	75	
Address setup time	t_{AS}		$t\phi - 40$	—	
Address hold time	t_{AH}		-8*2	—	
Instruction setup time	t_{IS}		60	—	
Instruction hold time	t_{IH}		-8*2	—	
Read data access time	t_{ACC}		—	$3t\phi - 120$	

Note: $t\phi = t_{cyc}/2$
*1: MSM66P573 = $2t\phi - 20$
*2: MSM66P573 = 0



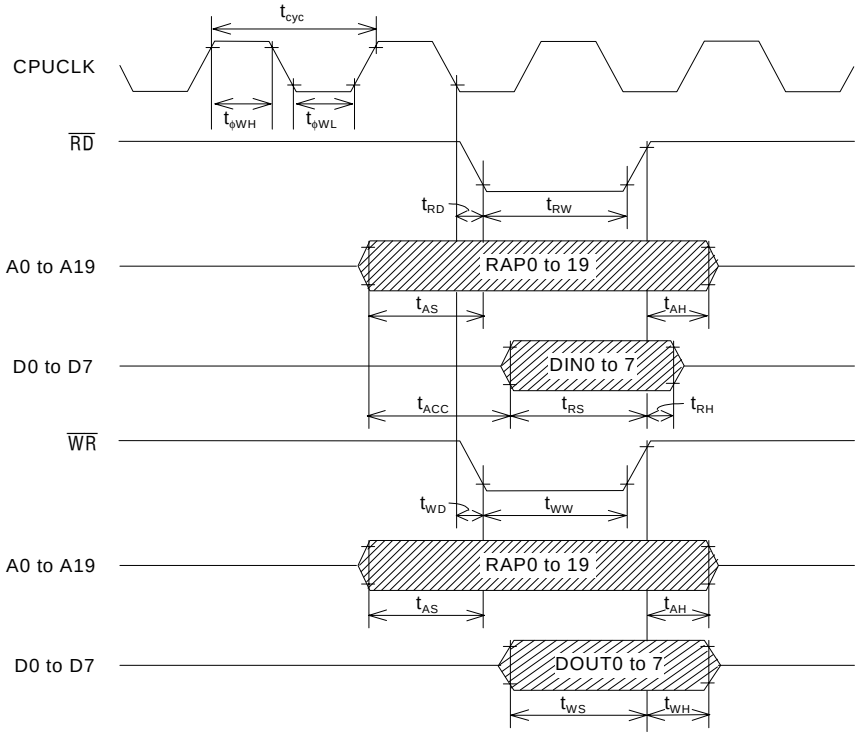
Bus timing during no wait cycle time

(2) External data memory control

MSM66573L/Q573L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q573LY (V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)
MSM66P573 (V_{DD} = 2.7 to 3.6 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{RD}$ pulse width	t_{RW}		2tϕ – 25*1	—	
$\overline{WR}$ pulse width	t_{WW}		2tϕ – 25*1	—	
$\overline{RD}$ pulse delay time	t_{RD}		—	75	
$\overline{WR}$ pulse delay time	t_{WD}		—	75	
Address setup time	t_{AS}		tϕ – 40	—	
Address hold time	t_{AH}		tϕ – 8*2	—	
Read data setup time	t_{RS}		60	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	3tϕ – 120	
Write data setup time	t_{WS}		2tϕ – 40*3	—	
Write data hold time	t_{WH}		tϕ – 6	—	

Note: tϕ = t_{cyc}/2
*1: MSM66P573 = 2 tϕ – 20
*1: MSM66Q573L/Q573LY = 2 tϕ – 30
*2: MSM66P573 = tϕ – 6
*3: MSM66Q573L/Q573LY = 2tϕ – 50



Bus timing during no wait cycle time

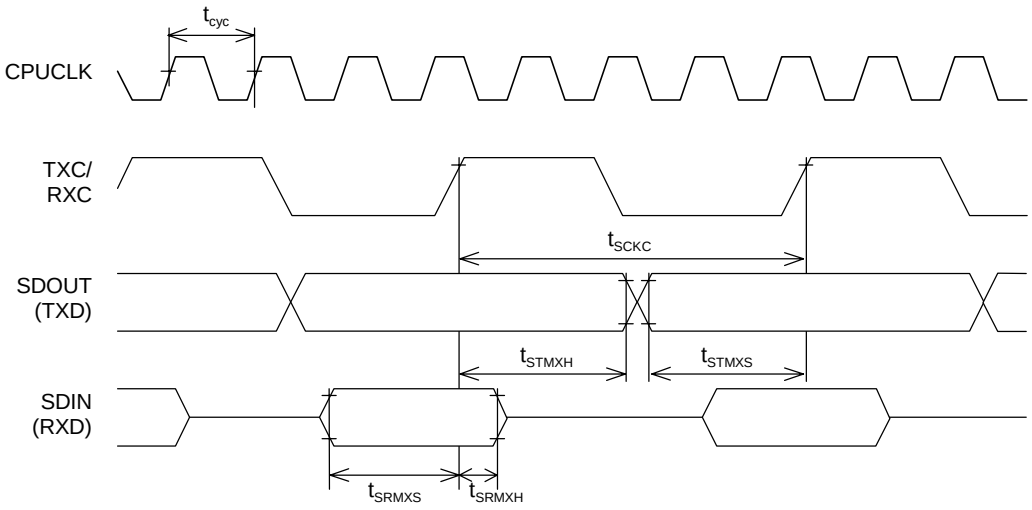
(3) Serial port control

Master mode

MSM66573L/Q573L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q573LY (V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)
MSM66P573 (V_{DD} = 2.7 to 3.6 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2tϕ – 10	—	
Output data hold time	t_{STMXH}		5tϕ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		0	—	

Note: tϕ = t_{cyc}/2

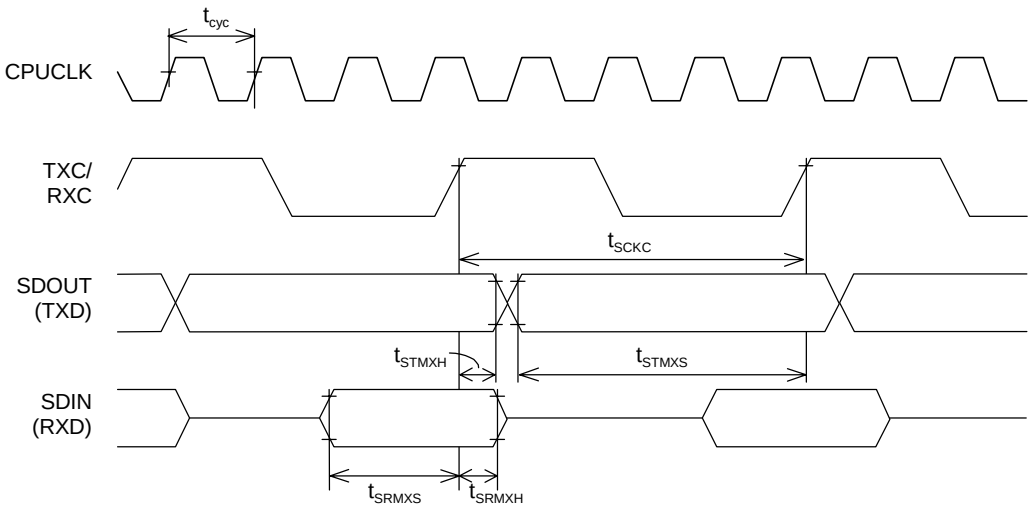


Slave mode

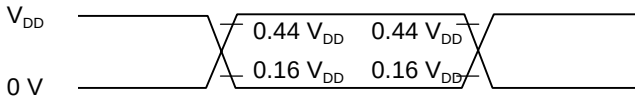
MSM66573L/Q573L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q573LY (V_{DD} = 2.7 to 3.3 V, Ta = –20 to +50°C)
MSM66P573 (V_{DD} = 2.7 to 3.6 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	$4t_{cyc}$	—	
Output data setup time	t_{STMXS}		$2t\phi - 30$	—	
Output data hold time	t_{STMXH}		$4t\phi - 20$	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		7	—	

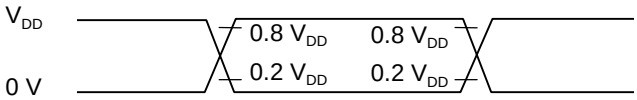
Note: $t\phi = t_{cyc}/2$



Measurement points for AC timing (except the serial port)



Measurement points for AC timing (the serial port)



A/D Converter Characteristics 1 (V_{DD} = 4.5 to 5.5 V)

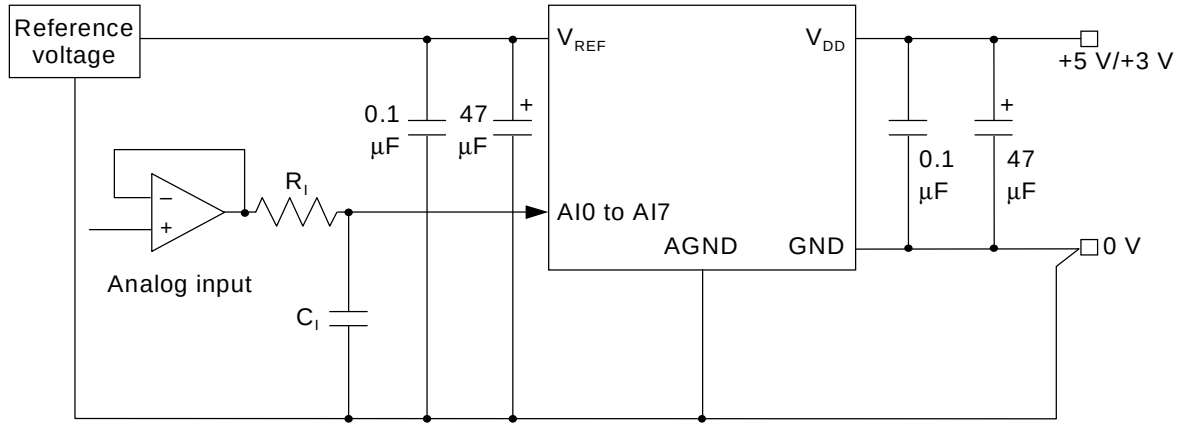
MSM6573/Q573/Q573Y/P573 (Ta = –30 to +70°C, V_{DD} = V_{REF} = 4.5 to 5.5 V, AGND = GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_I \leq 5$ kΩ t_{CONV} = 10.7 µs	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential Linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit 2	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	10.7	—	3906.3	µs/ch

A/D Converter Characteristics 2 (V_{DD} = 2.4 to 3.6 V)

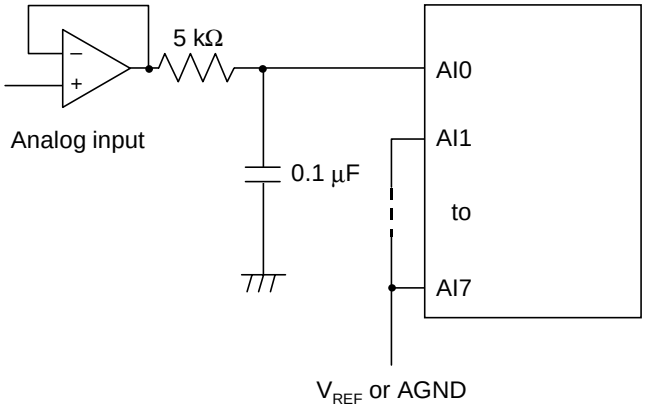
MSM66573L/Q573L (Ta = –30 to +70°C, V_{DD} = V_{REF} = 2.4 to 3.6 V, AGND = GND = 0 V)
MSM66Q573LY (Ta = –20 to +50°C, V_{DD} = V_{REF} = 2.7 to 3.3 V, AGND = GND = 0 V)
MSM66P573 (Ta = –30 to +70°C, V_{DD} = V_{REF} = 2.7 to 3.6 V, AGND = GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_I \leq 5$ kΩ t_{CONV} = 27.4 µs	—	10	—	Bit
Linearity error	E_L		—	—	±4	LSB
Differential Linearity error	E_D		—	—	±3	
Zero scale error	E_{ZS}		—	—	+4	
Full-scale error	E_{FS}		—	—	–4	
Cross talk	E_{CT}	Refer to measurement circuit 2	—	—	±2	
Conversion time	t_{CONV}	Set according to ADTM set data	27.4	—	3906.3	µs/ch



R_I (impedance of analog input source) ≤ 5 kΩ
$C_I \cong 0.1$ µF

Measurement Circuit 1



Cross talk is the difference between the A/D conversion results when the same analog input is applied to AI0 through AI7 and the A/D conversion results of the circuit to the left.

Measurement Circuit 2

Definition of Terminology

1. Resolution
   Resolution is the value of minimum discernible analog input.
   With 10 bits, since $2^{10} = 1024$, resolution of $(V_{REF} - AGND) \div 1024$ is possible.

2. Linearity error
   Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of a 10-bit A/D converter (not including quantization error).
   Ideal conversion characteristics can be obtained by dividing the voltage between V_{REF} and AGND into 1024 equal steps.

3. Differential linearity error
   Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1 converted bit of digital output is $1LSB = (V_{REF} - AGND) \div 1024$. Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

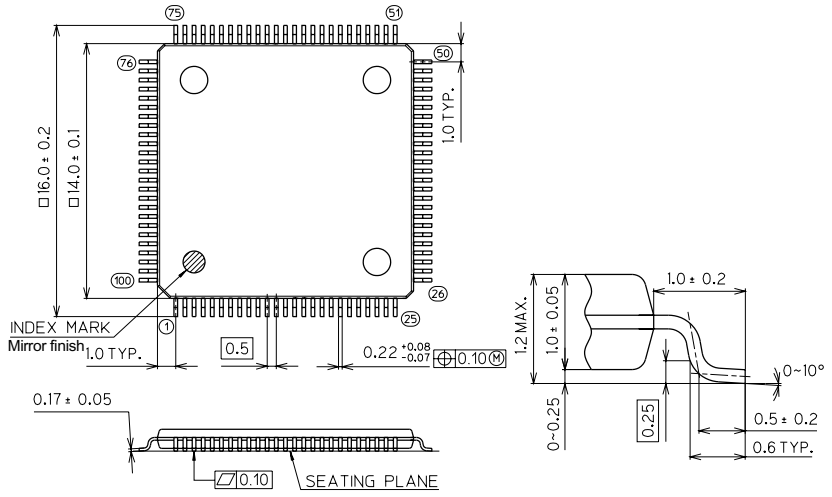
4. Zero scale error
   Zero scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 000H to 001H.

5. Full-scale error
   Full-scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 3FEH to 3FFH.

PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

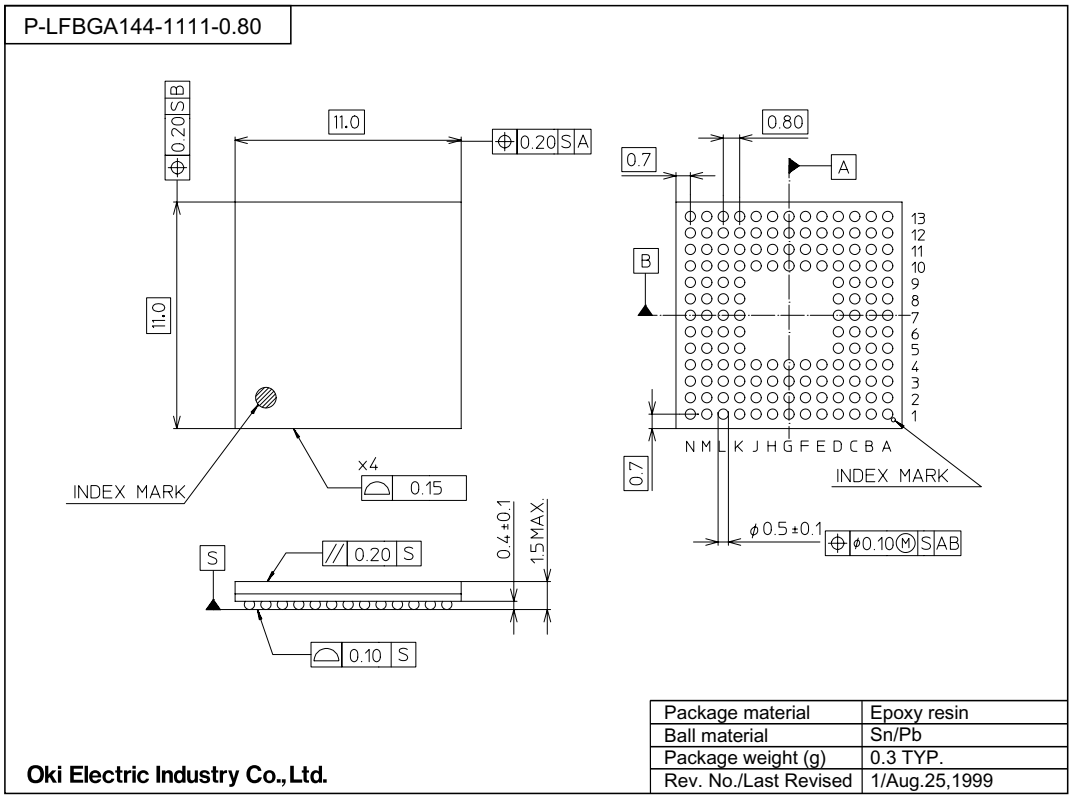
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

PACKAGE DIMENSIONS

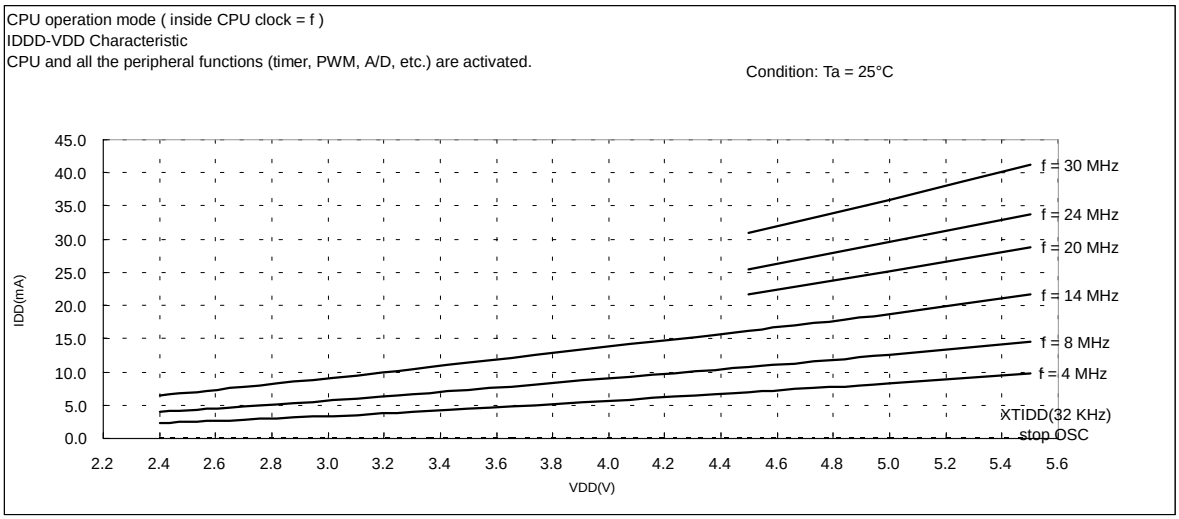
(Unit: mm)



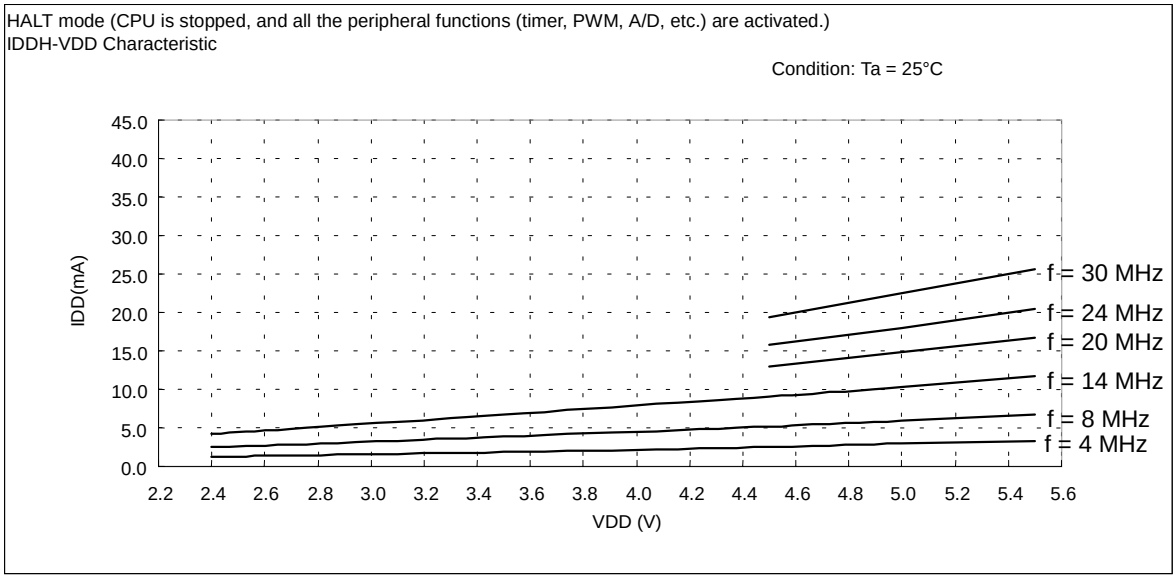
Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REFERENCE DATA

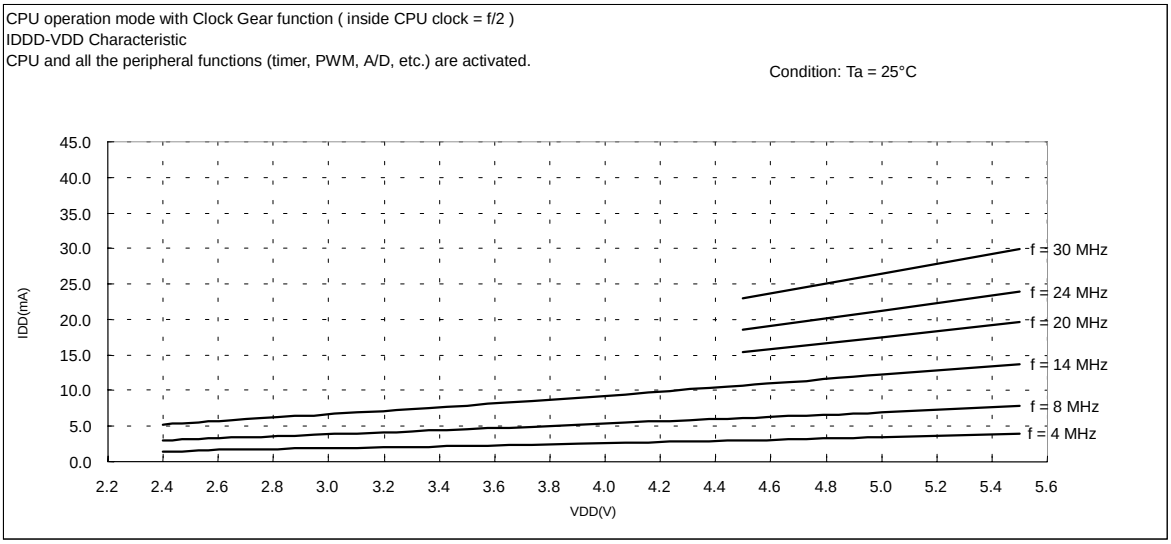


	VDD	2.4 V	2.7 V	3.3 V	4.5 V	5.0 V	5.5 V
IDDD (mA)	30 MHz				30.8725	35.8775	41.1125
	24 MHz				25.4675	29.6225	33.8025
	20 MHz				21.7525	25.2125	28.8075
	14 MHz	6.5325	7.74	10.3675	16.175	18.7775	21.6175
	8 MHz	4.005	4.8175	6.56	10.6975	12.5475	14.4825
	4 MHz	2.2875	2.815	4.03	7.02	8.3525	9.7575
	32.768 kHz	0.023	0.027	0.032	0.052	0.056	0.062

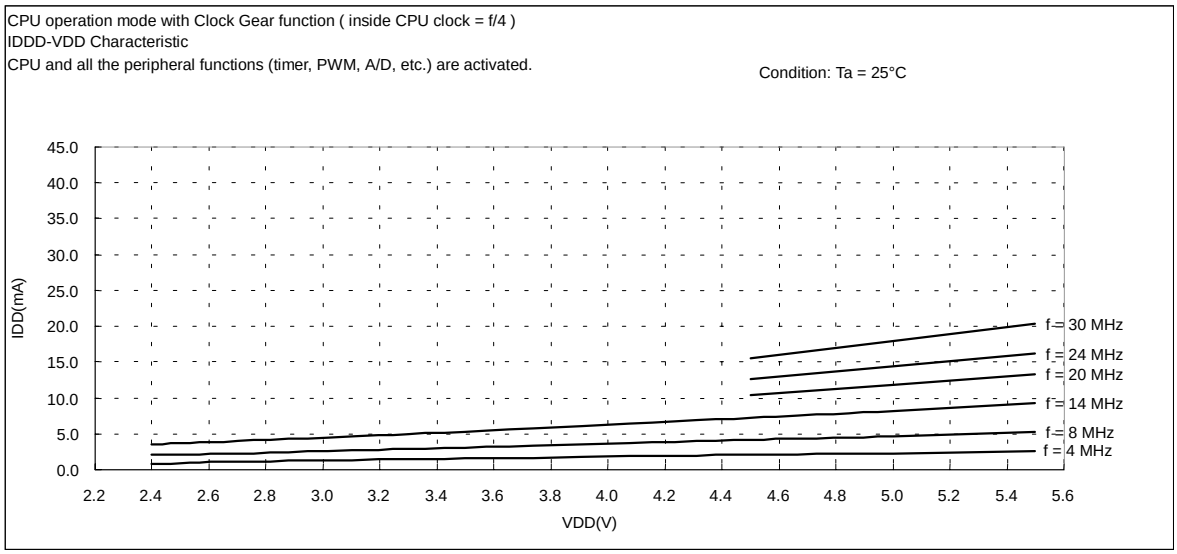


	VDD	2.4 V	2.7 V	3.3 V	4.5 V	5.0 V	5.5 V
IDDH (mA)	30 MHz				19.43346	22.48822	25.61874
	24 MHz				15.74174	18.04172	20.41748
	20 MHz				13.01898	14.86622	16.79474
	14 MHz	4.213	4.8715	6.1825	9.0595	10.34548	11.69122
	8 MHz	2.442	2.79	3.52275	5.155	5.88725	6.65175
	4 MHz	1.20025	1.37975	1.74175	2.54925	2.9115	3.2955

REFERENCE DATA



	VDD	2.4 V	2.7 V	3.3 V	4.5 V	5.0 V	5.5 V
IDDD (mA)	30 MHz				23.04622	26.44046	29.93146
	24 MHz				18.56048	21.17448	23.84848
	20 MHz				15.3537	17.45246	19.62772
	14 MHz	5.1845	5.93925	7.43425	10.73924	12.21222	13.74696
	8 MHz	2.994	3.39625	4.2425	6.11975	6.96425	7.83525
	4 MHz	1.48	1.68175	2.0975	3.03325	3.4465	3.88425



	VDD	2.4 V	2.7 V	3.3 V	4.5 V	5.0 V	5.5 V
IDDD (mA)	30 MHz				15.51348	17.90122	20.32898
	24 MHz				12.60374	14.36524	16.19224
	20 MHz				10.40248	11.81124	13.26998
	14 MHz	3.483	4.00875	5.0365	7.25025	8.23925	9.27275
	8 MHz	2.0285	2.3035	2.8735	4.12475	4.691	5.276
	4 MHz	0.796	1.1355	1.416	2.036	2.3155	2.60175

REVISION HISTORY

Date	Changes compared to previous version
Mar. 2000	-
Oct. 2000	- Modified the contents of FEATURES “Timers and A/D converter“ on P-2. - Modified the contents of PIN DESCRIPTIONS “P3_2/$\overline{RD}$ and P3_3/$\overline{WR}$ Secondary function” on P-7. - Added the contents of PIN DESCRIPTIONS “V_{REF} and AGND Description” on P-9. - Changed the contents of ABSOLUTE MAXIMUM RATINGS “Digital power supply voltage Condition and Rating” on P-10. - Changed the contents of RECOMMENDED OPERATING CONDITIONS “Memory hold voltage Condition and Rating” on P-10. - Changed the contents of DC Characteristics 2 “H input voltage Min. value” on P-14. - Changed the contents of Measurement points for AC timing on P-23. - Changed the contents of A/D Converter Characteristics 1 and 2 “Conversion time Max. value” on P-24.
Feb. 2001	- Changed the name from “MSM66Q573LY” to “MSM66Q573L” on P-1 to P-3. - Changed the name from “MSM66Q573Y” to “MSM66Q573” on P-1 to P-3. - Changed the voltage value from “2.7 to 3.3V” to “2.4 to 3.6V” on P-1 and P-3. - Added the MSM66Q573 in ABSOLUTE MAXIMUM RATINGS and RECOMMENDED OPERATING CONDITIONS on P-10. - Added the MSM66Q573L in ABSOLUTE MAXIMUM RATINGS and RECOMMENDED OPERATING CONDITIONS on P-10. - Added the MSM66Q573 in ALOWABLE OUTPUT CURRENT VALUES and INTERNAL FLASH ROM PROGRAMMING CONDITIONS on P-11. - Added the MSM66Q573L in ALOWABLE OUTPUT CURRENT VALUES and INTERNAL FLASH ROM PROGRAMMING CONDITIONS on P-11. - Added the MSM66Q573 condition top of the table on P-12. - Modified the mark of “f” to “f_{XT}” and “f_{OSC}” on P-12 to P15. - Changed the Supply current value of MSM66Q573Y f_{XT} = 32.768kHz on P-13. - Added the Supply current value of MSM66Q573 on P-13. - Added the MSM66Q573L condition above the table on P-14. - Changed the Supply current value of MSM66Q573LY f_{XT} = 32.768kHz on P-15. - Added the Supply current value of MSM66Q573L on P-15. - Added the MSM66Q573 condition top of the table on P-16 to P-19. - Added the MSM66Q573L condition top of the table on P-20 to P-23. - Added the MSM66Q573L condition bottom of the table on P-21. - Added conditions top of the A/D Converter Characteristics 1 table on P-24. - Added the MSM66Q573L condition top of the A/D Converter Characteristics 2 table on P-24.
May. 2001	- Changed the value of MSM66Q573Y Supply current on P-13. - Changed the value of MSM66Q573LY Supply current on P-15. - Added the REFERENCE DATA on P-28. - The OTP ROM product has been removed from P-1 and P-2.

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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