NEC

MOS INTEGRATED CIRCUIT
μPD3728DZ

7300 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD3728DZ is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD3728DZ has 3 rows of 7300 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 7300 pixels separately in odd and even pixels. Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers and so on.

FEATURES

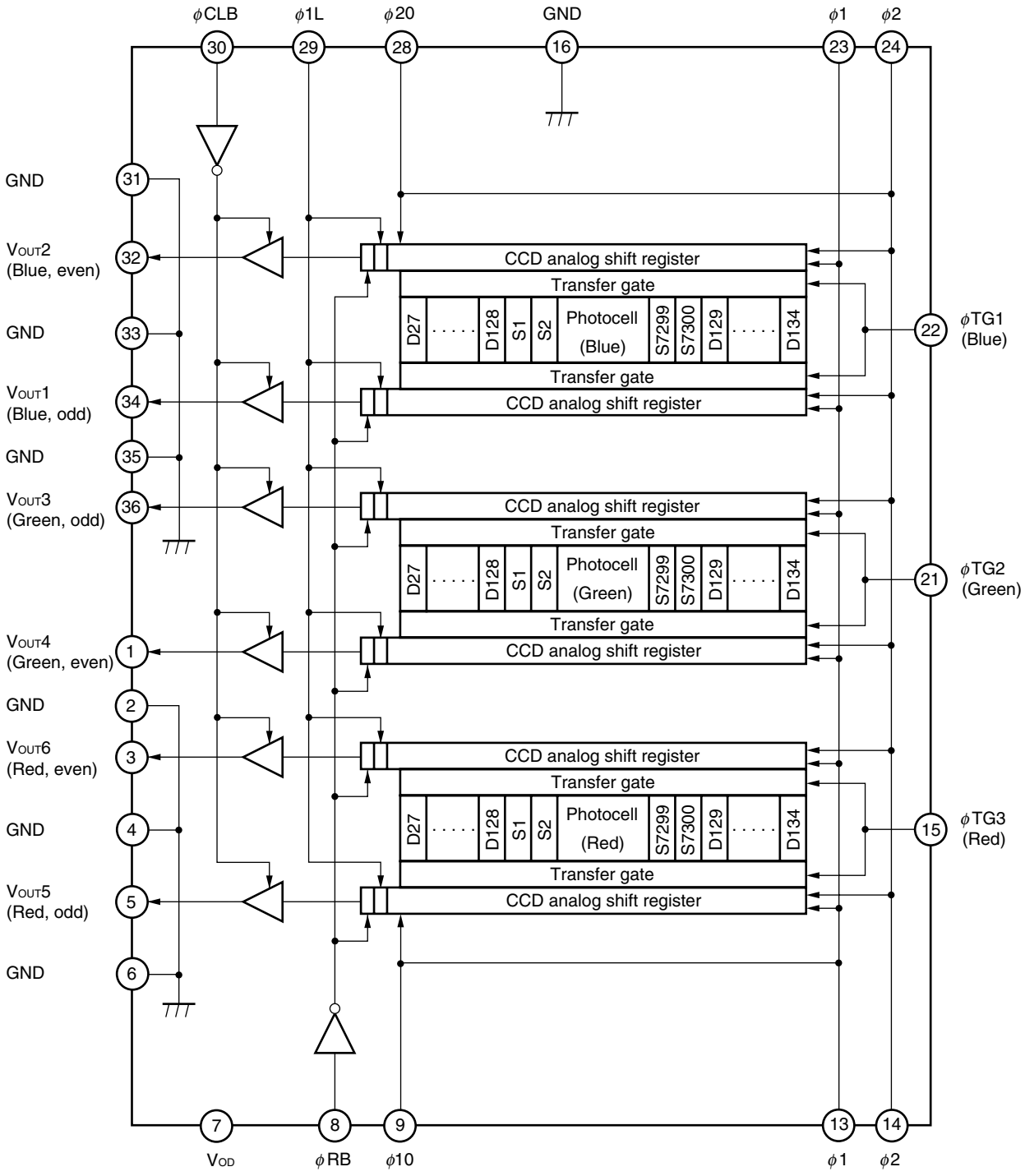
- Valid photocell : 7300 pixels × 3
- Photocell pitch : 10 μm
- Line spacing : 40 μm (4 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 24 dot/mm A3 (297 × 420 mm) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 40 MHz MAX. (20 MHz/1 output)
- Output type : 2 outputs in phase/color
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD3728DZ	CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

Document No. S15417EJ1V0DS00 (1st edition)
Date Published July 2001 NS CP (K)
Printed in Japan

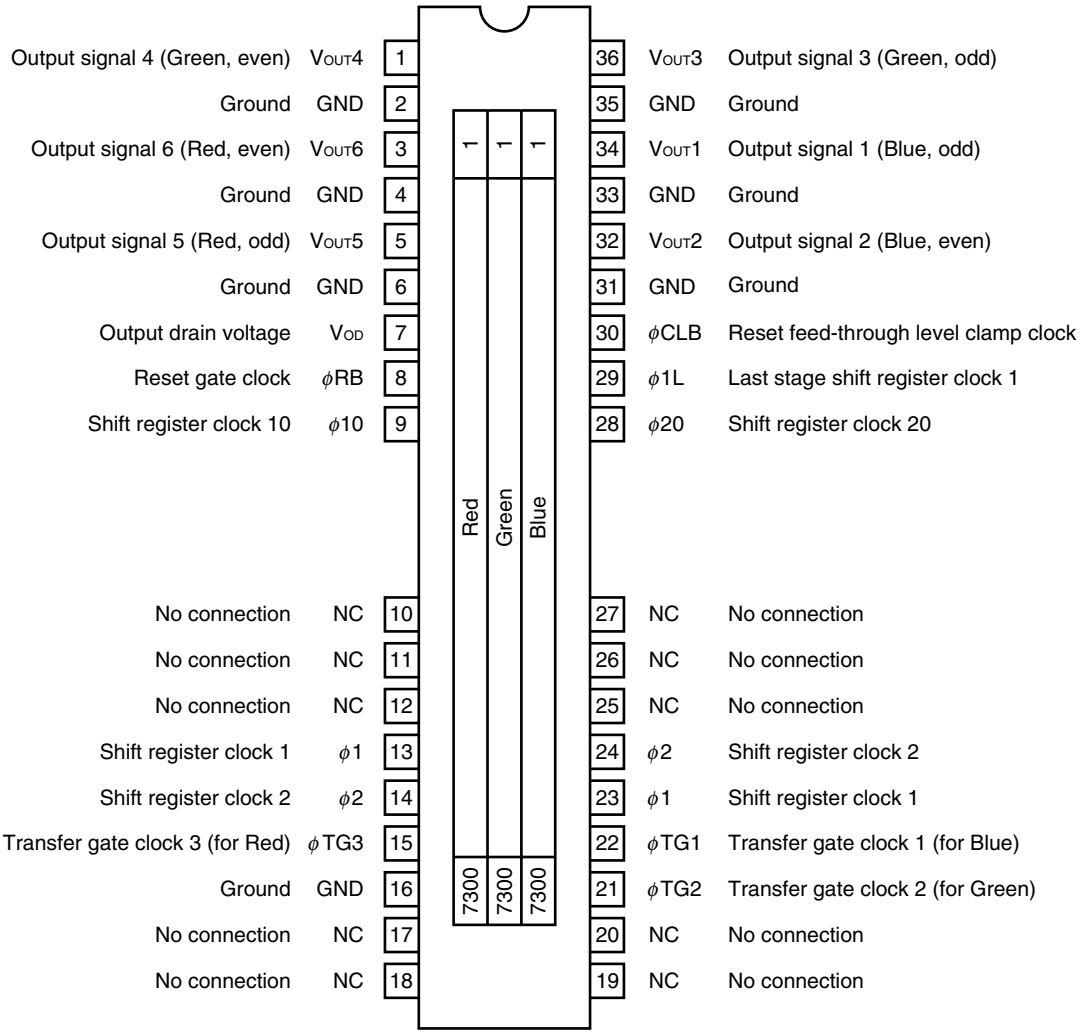
BLOCK DIAGRAM



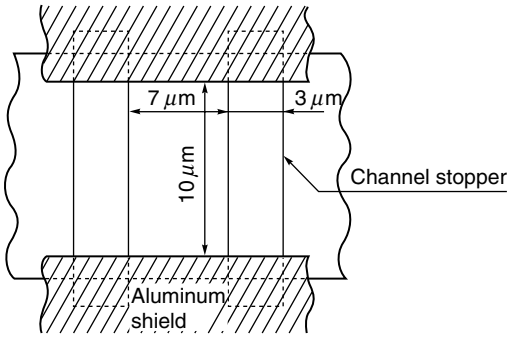
PIN CONFIGURATION (Top View)

CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

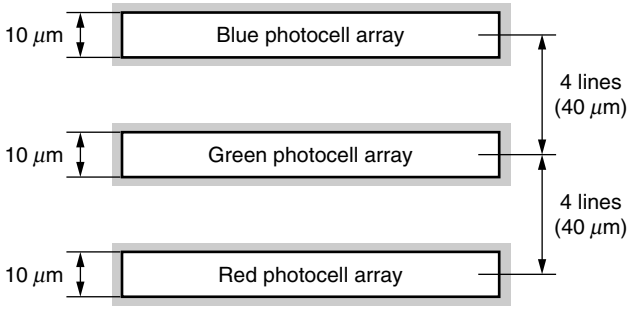
• μPD3728DZ



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 1L}$, $V_{\phi 10}$, $V_{\phi 2}$, $V_{\phi 20}$	−0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	−0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	−0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	−0.3 to +8	V
Operating ambient temperature	T_A	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 1LH}$, $V_{\phi 10H}$, $V_{\phi 2H}$, $V_{\phi 20H}$	4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 1LL}$, $V_{\phi 10L}$, $V_{\phi 2L}$, $V_{\phi 20L}$	−0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	−0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	−0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.5	$V_{\phi 1H}$ Note ($V_{\phi 10H}$)	$V_{\phi 1H}$ Note ($V_{\phi 10H}$)	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	−0.3	0	+0.5	V
Data rate	$2f_{\phi RB}$	−	2	40	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than Shift register clock high level ($V_{\phi 1H}$ ($V_{\phi 10H}$)), Image lag can increase.

Remark Pin 9 (ϕ10) and pin 28 (ϕ20) should be open to decrease the influence of input clock noise to output signal waveform, in case of operating at low or middle speed range; data rate under 24 MHz or so.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{OD} = 12 V, $f_{\phi RB}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p}, light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1 mm)+HA-50 (heat absorbing filter, t = 3 mm)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}		1.5	2.0	–	V
Saturation exposure	Red	SER		–	0.35	–	lx•s
	Green	SEG		–	0.39	–	lx•s
	Blue	SEB		–	0.31	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6.0	18.0	%
Average dark signal Note1		ADS1	Light shielding	–	1.0	5.0	mV
		ADS2		–	0.5	5.0	mV
Dark signal non-uniformity Note1		DSNU1	Light shielding	–	2.0	5.0	mV
		DSNU2		–	1.0	5.0	mV
Power consumption		P_W		–	600	800	mW
Output impedance		Z_O		–	0.3	0.5	kΩ
Response	Red	R_R		3.9	5.6	7.3	V/lx•s
	Green	R_G		3.6	5.1	6.6	V/lx•s
	Blue	R_B		4.5	6.4	8.3	V/lx•s
Image lag Note1		IL1	V_{OUT} = 1.0 V	–	2.0	5.0	%
		IL2		–	1.0	5.0	%
Offset level Note2		V_{OS}		4.0	5.0	6.0	V
Output fall delay time Note3		t_d	V_{OUT} = 1.0 V	–	20	–	ns
Register imbalance		RI	V_{OUT} = 1.0 V	0	–	4.0	%
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 40 MHz	95	98	–	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	460	–	nm
Dynamic range Note1		DR11	V_{sat}/DSNU1	–	1000	–	times
		DR12	V_{sat}/DSNU2	–	2000	–	times
		DR21	V_{sat}/σbit1	–	2000	–	times
		DR22	V_{sat}/σbit2	–	4000	–	times
Reset feed-through noise Note2		RFTN	Light shielding	–500	+200	+500	mV
Random noise Note1		σbit1	Light shielding,	–	1.0	–	mV
		σbit2	bit clamp mode (t_{cp} = 150 ns)	–	0.5	–	mV
		σline1	Light shielding,	–	4.0	–	mV
		σline2	line clamp mode (t19 = 3 μs)	–	2.0	–	mV

Notes 1. ADS1, DSNU1, IL1, DR11, DR21, σbit1 and σline1 show the specification of V_{OUT}1 and V_{OUT}2. ADS2, DSNU2, IL2, DR12, DR22, σbit2 and σline2 show the specification of V_{OUT}3 to V_{OUT}6.

2. Refer to **TIMING CHART 2, 5**.

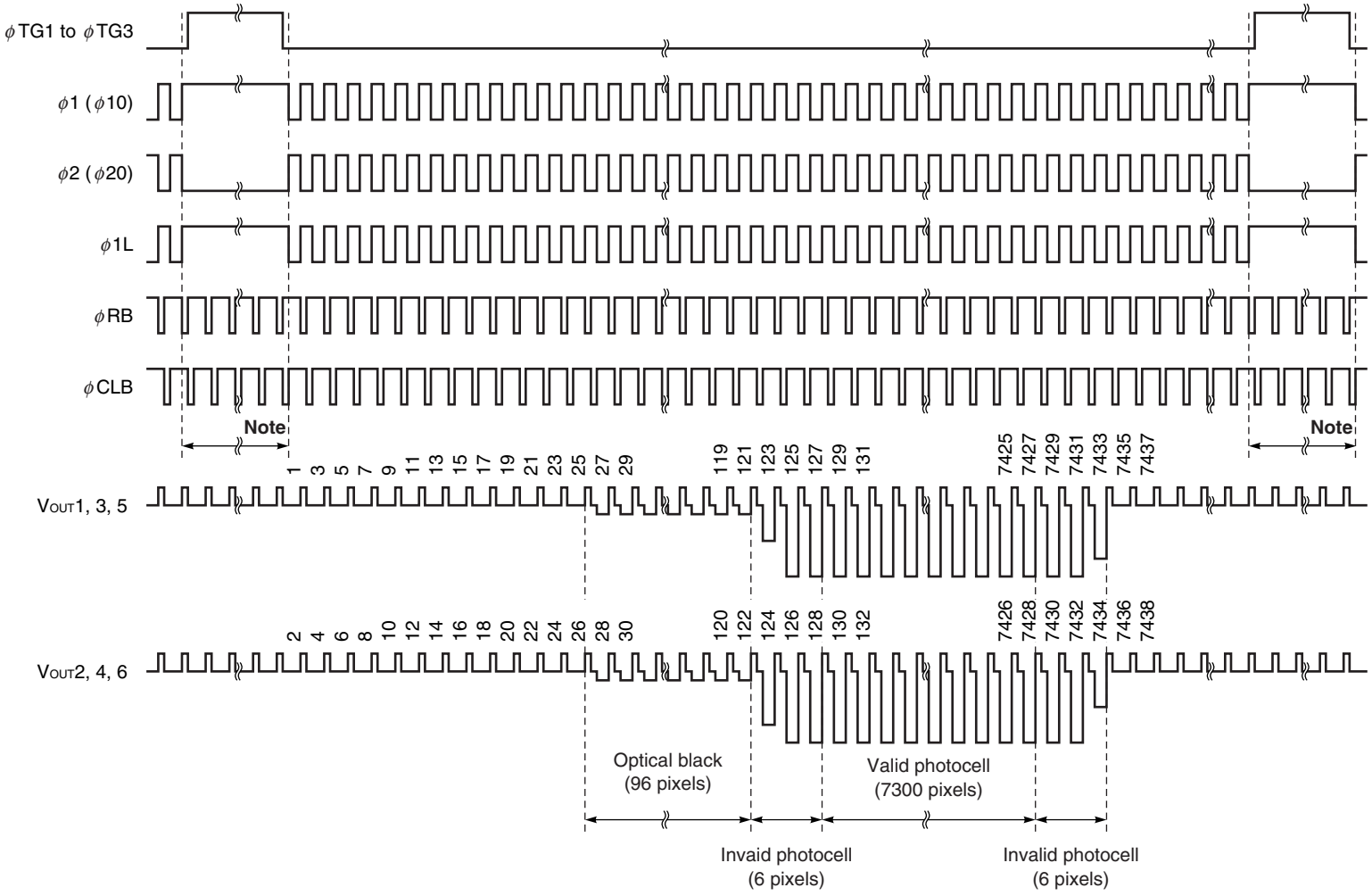
3. When the fall time of ϕ1L (t2') is the TYP. value (refer to **TIMING CHART 2, 5**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	13	–	350	500	pF
			23	–	350	500	pF
		ϕ10	9	–	350	500	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	14	–	350	500	pF
			24	–	350	500	pF
		ϕ20	28	–	350	500	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ1L	29	–	10	–	pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	8	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	30	–	10	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG1	22	–	100	–	pF
		ϕTG2	21	–	100	–	pF
		ϕTG3	15	–	100	–	pF

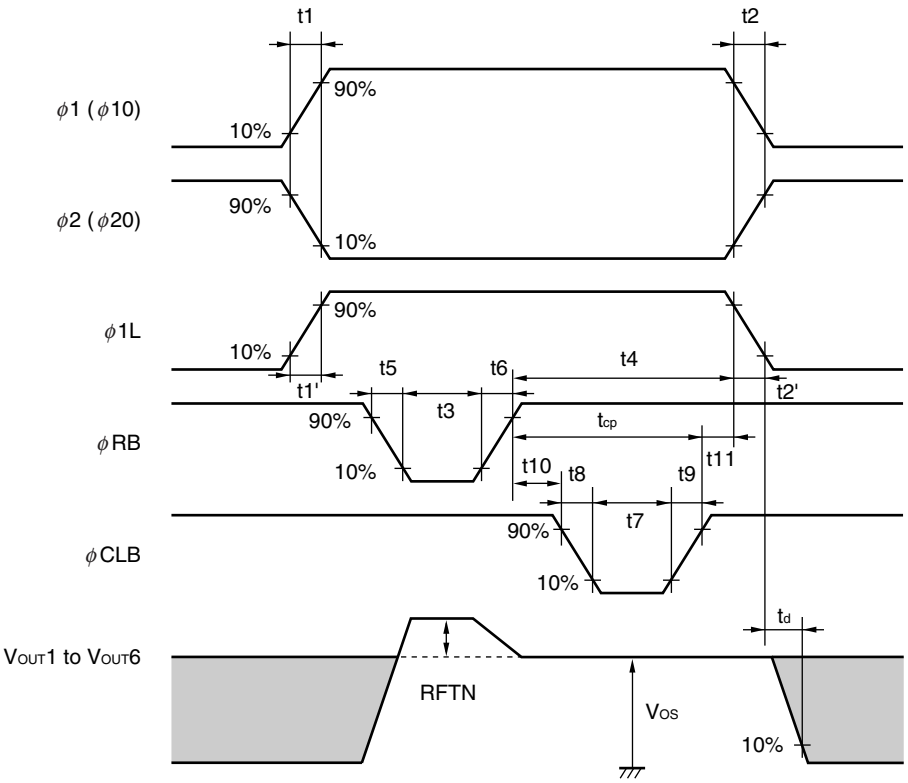
Remark Pins 13, 23 (ϕ1) and pin 9 (ϕ10) are connected each other inside of the device.
Pins 14, 24 (ϕ2) and pin 28 (ϕ20) are connected each other inside of the device.

TIMING CHART 1 (Bit clamp mode, for each color)



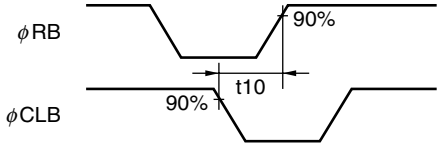
Note Input the φRB and φCLB pulses continuously during this period, too.

TIMING CHART 2 (Bit clamp mode, for each color)

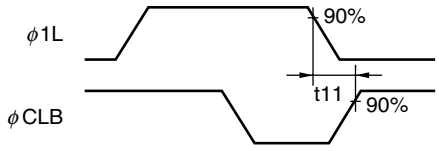


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	17	50	–	ns
t4	5	200	–	ns
t5, t6	0	20	–	ns
t7	17	150	–	ns
t8, t9	0	20	–	ns
t10	–10 Note 1	+50	–	ns
t11	–5 Note 2	+50	–	ns
t_{cp}	5	150	–	ns

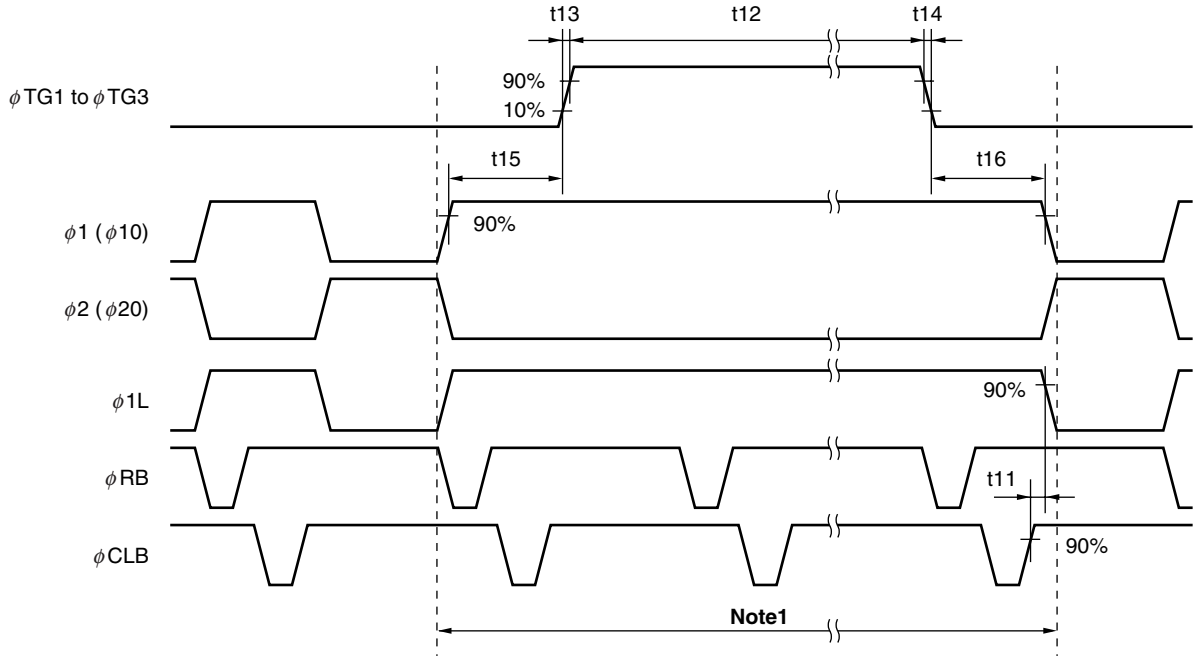
Notes 1. Min. of t10 shows that the φRB and φCLB overlap each other.



2. Min. of t11 shows that the φ1L and φCLB overlap each other.



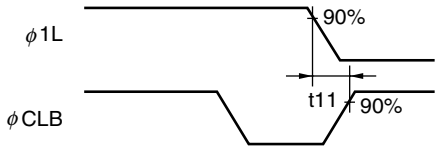
TIMING CHART 3 (Bit clamp, for each color)



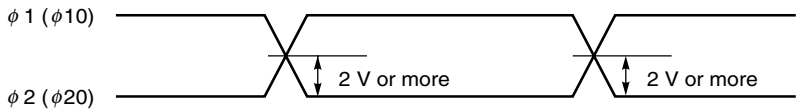
Symbol	Min.	Typ.	Max.	Unit
t11	−5 Note 2	+50	−	ns
t12	3000	10000	−	ns
t13, t14	0	50	−	ns
t15, t16	900	1000	−	ns

Notes 1. Input the φRB and φCLB pulses continuously during this period, too.

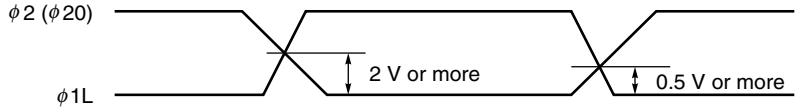
2. Min. of t11 shows that the φ1L and φCLB overlap each other.



φ1 (φ10), φ2 (φ20) cross points

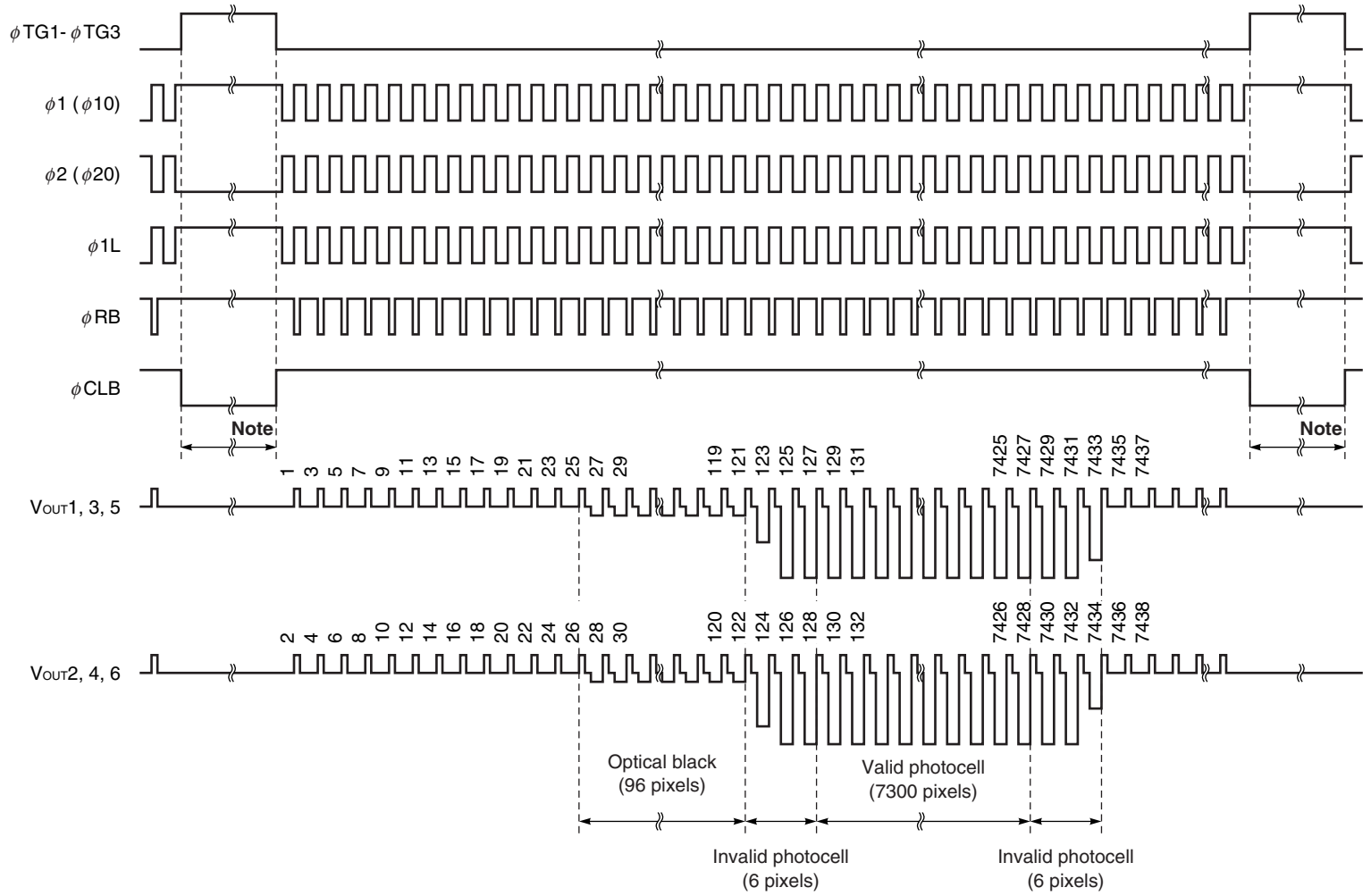


φ1L, φ2 (φ20) cross points



Remark Adjust cross points (φ1 (φ10), φ2 (φ20)) and (φ1L, φ2 (φ20)) with input resistance of each pin.

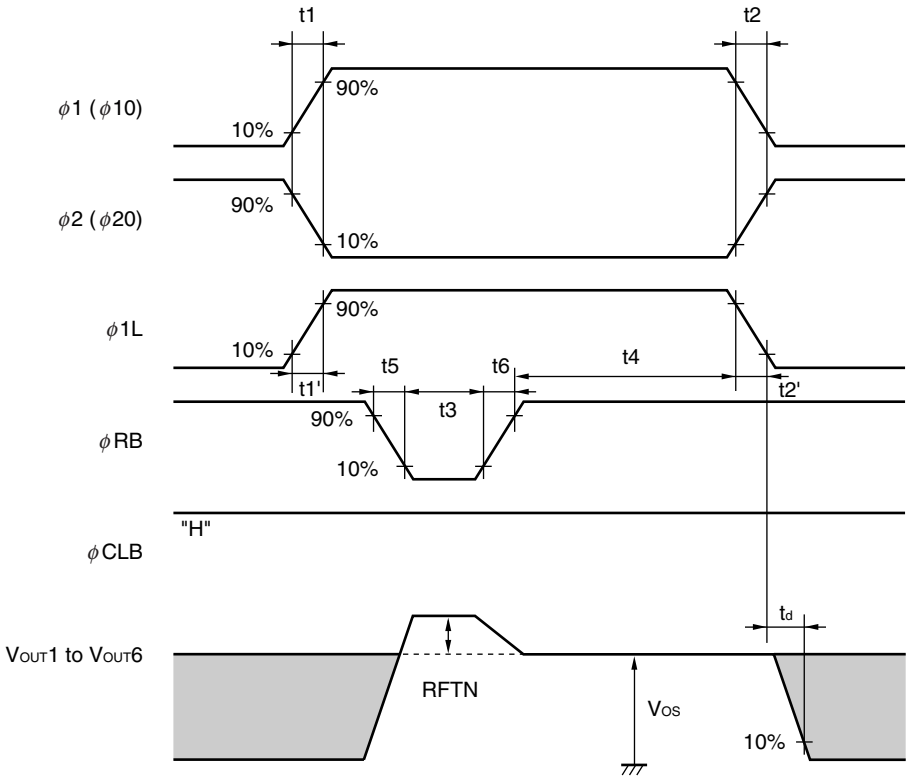
TIMING CHART 4 (Line clamp mode, for each color)



Note Set the φRB pulse to high level during this period.

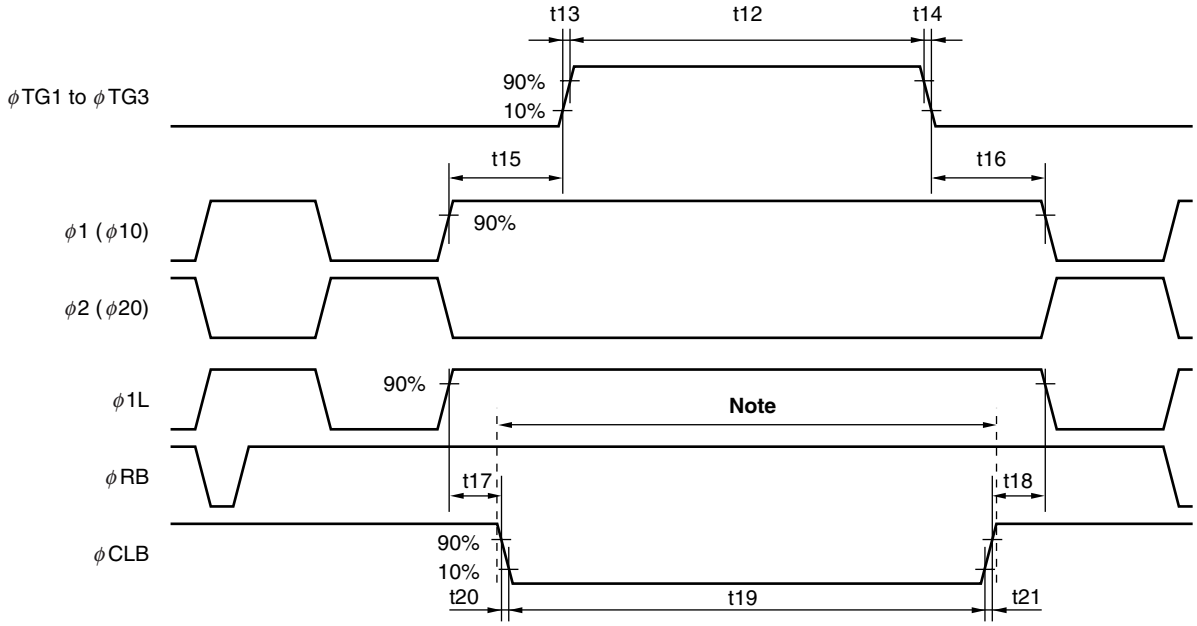
Remark Inverse pulse of φTG1 to φTG3 can be used as φCLB.

TIMING CHART 5 (Line clamp mode, for each color)



Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	17	50	–	ns
t4	5	200	–	ns
t5, t6	5	20	–	ns

TIMING CHART 6 (Line clamp mode, for each color)

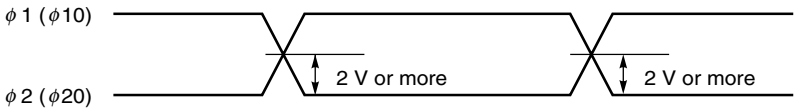


Symbol	Min.	Typ.	Max.	Unit
t12	3000	10000	–	ns
t13, t14	0	50	–	ns
t15, t16	900	1000	–	ns
t17, t18	100	1000	–	ns
t19	200	t12	–	ns
t20, t21	0	20	–	ns

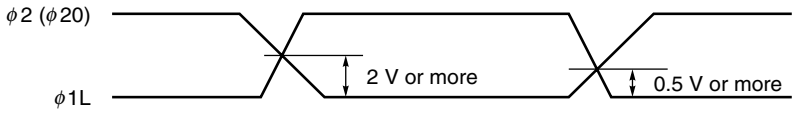
Note Set the φRB pulse to high level during this period.

Remark Inverse pulse of the φTG1 and φTG3 can be used as φCLB.

φ1 (φ10), φ2 (φ20) cross points



φ1L, φ2 (φ20) cross points



Remark Adjust cross points (φ1 (φ10), φ2 (φ20)) and (φ1L, φ2 (φ20)) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

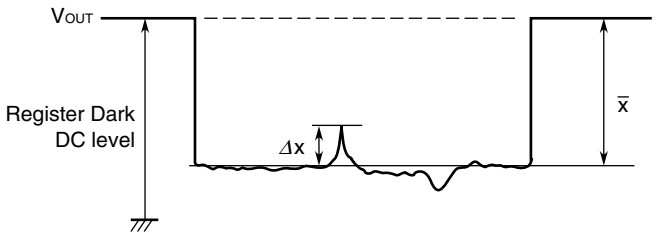
3. Photo response non-uniformity : **PRNU**
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{7300} x_j}{7300}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{7300} d_j}{7300}$$

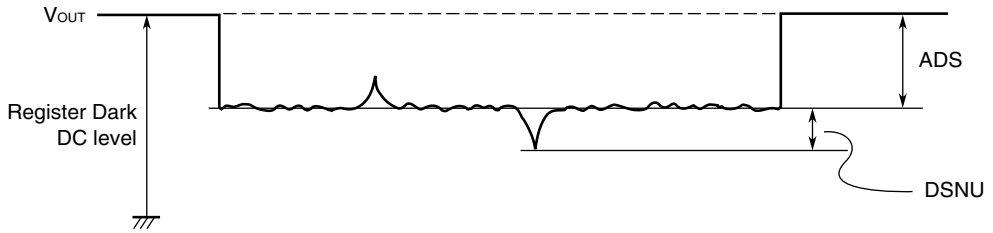
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}|_{j = 1 \text{ to } 7300}$$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

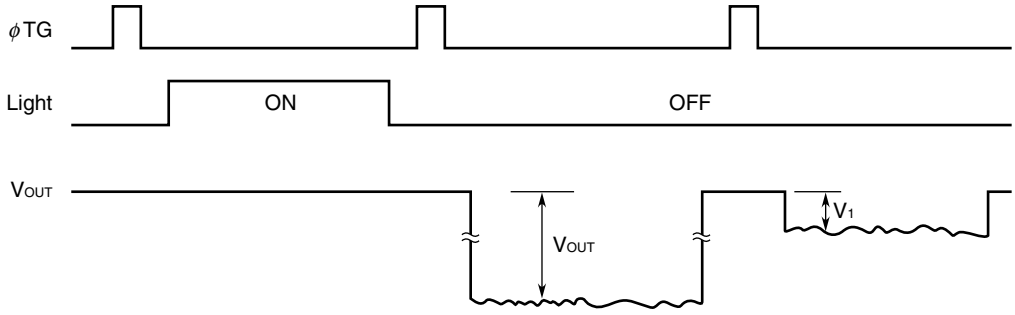
7. Response : **R**

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{OUT}} \times 100$$

9. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels. This is calculated by the following formula.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

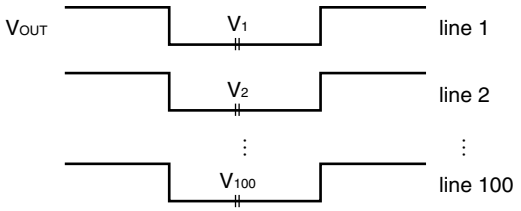
n : Number of valid pixels
V_j : Output voltage of each pixel

10. Random noise : $\boldsymbol{\sigma}$

Random noise is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). This is calculated by the following formula.

$$\sigma\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}}, \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

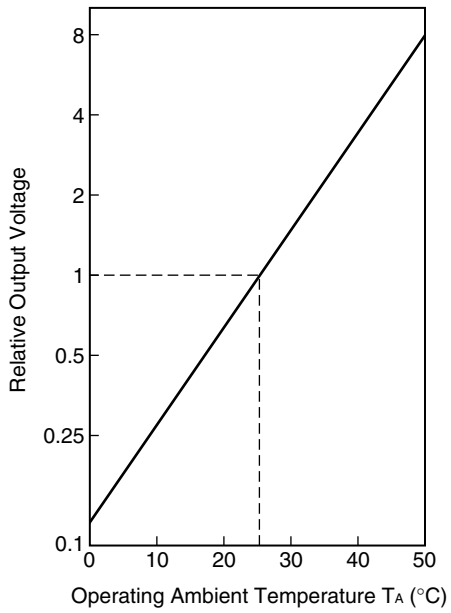
V_i : A valid pixel output signal among all of the valid pixels for each color



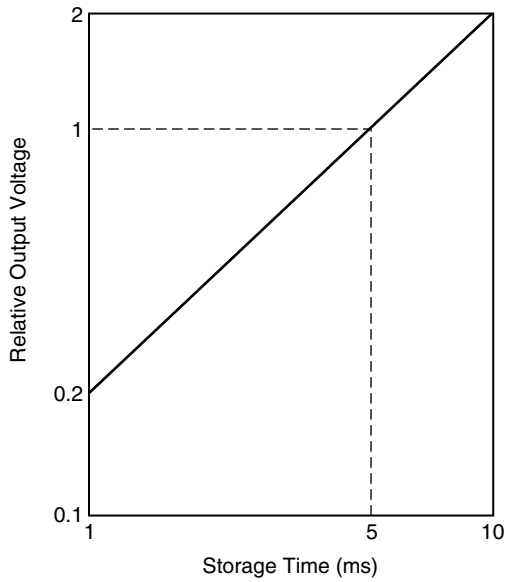
This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES (Nominal)

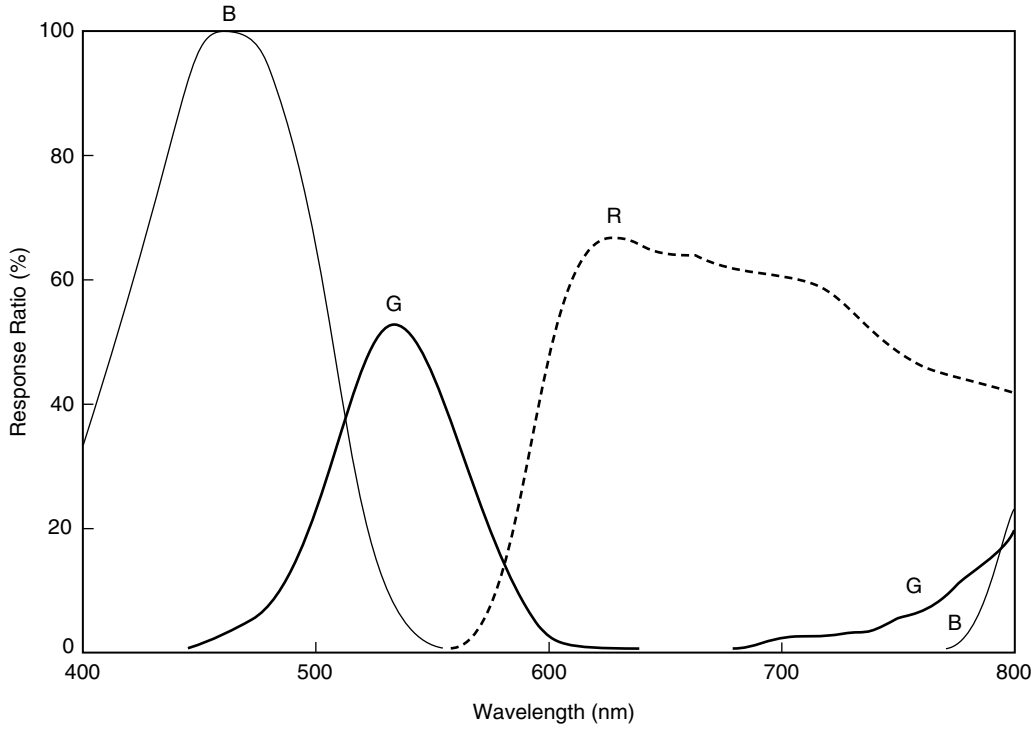
DARK OUTPUT TEMPERATURE CHARACTERISTIC



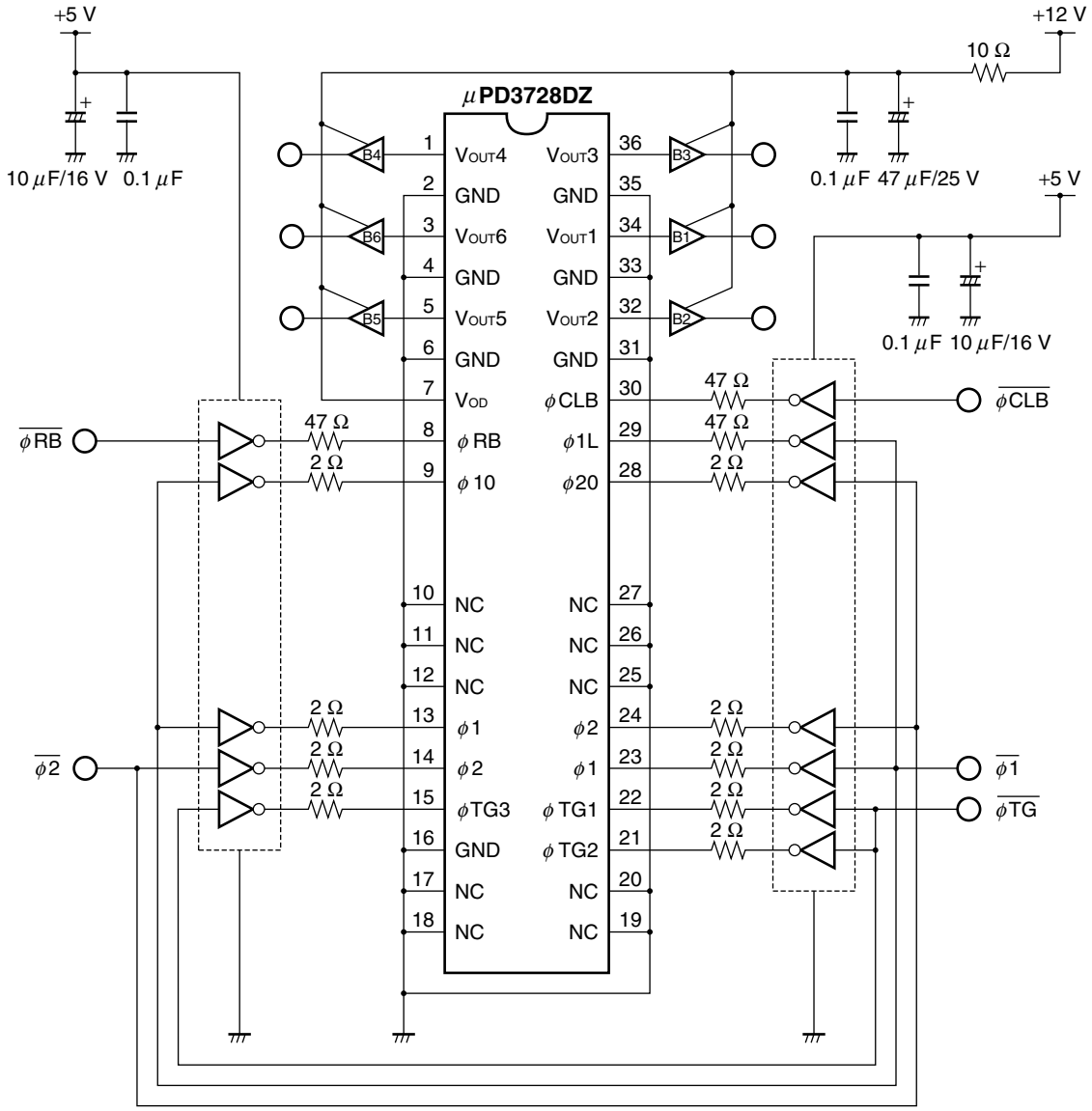
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (T_A = +25°C)



APPLICATION CIRCUIT EXAMPLE

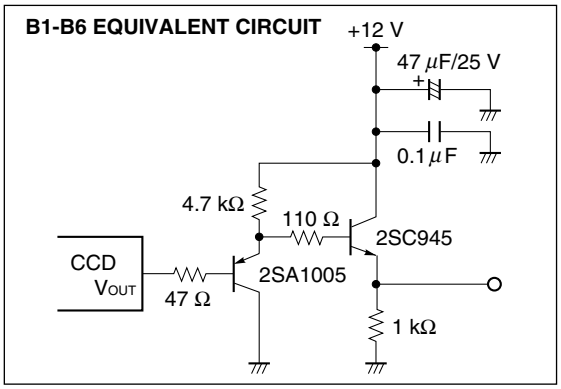


Remarks 1. Pin 9 (ϕ10) and pin 28 (ϕ20) should be open to decrease the influence of input clock noise to output signal waveform, in case of operating at low or middle speed range; data rate under 24 MHz or so.

2. Inverters shown in the above application circuit example are the 74AC04.

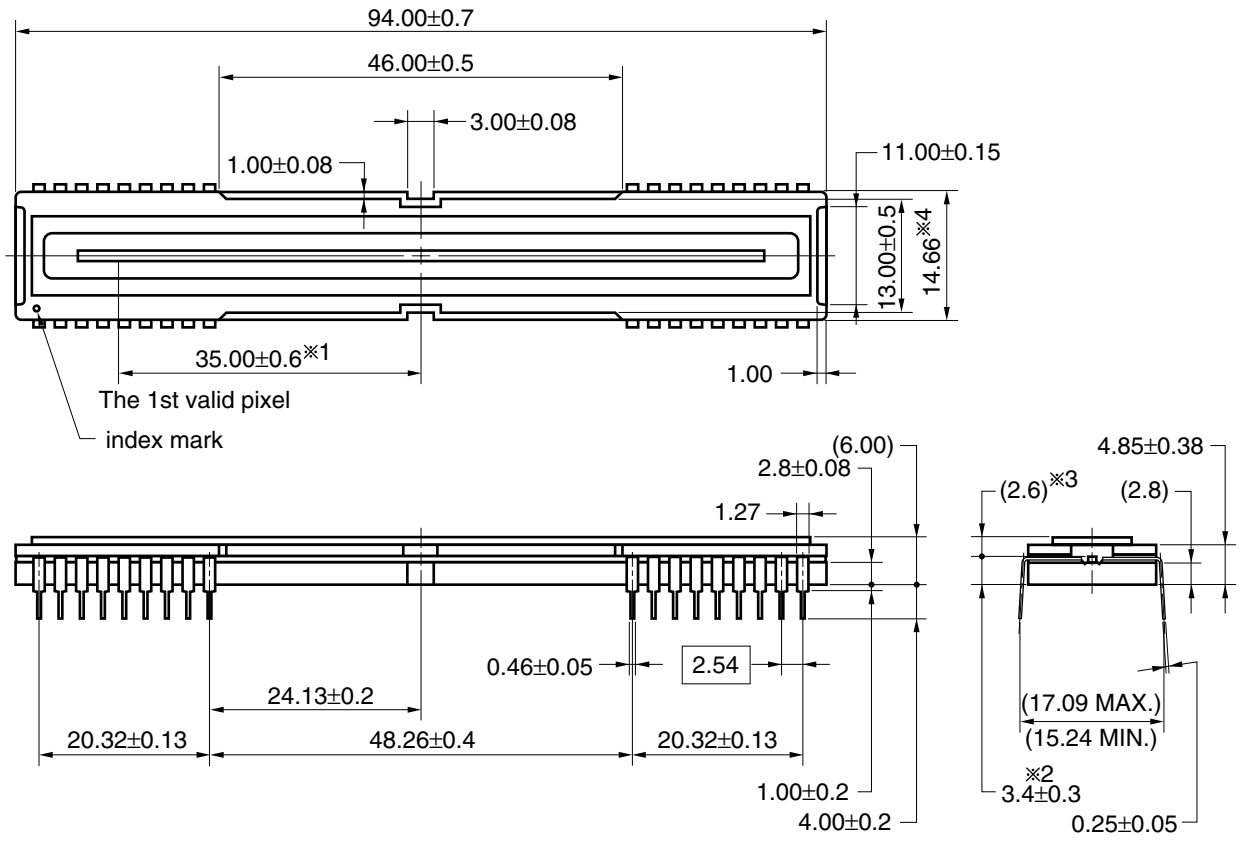
3. B1 to B6 in the application circuit example are shown in the figure below.

B1-B6 EQUIVALENT CIRCUIT



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 36-PIN CERAMIC DIP (15.24 mm (600))



Name	Dimensions	Refractive index
Glass cap	93.0 × 9.0 × 1.1	1.5

※1 1st valid pixel ←→ Center of package
※2 The bottom of package ←→ The surface of the chip
※3 The surface of the chip ←→ The surface of the glass cap
※4 The tolerance of package dimension
±0.25 : less than 10mm from W/F edge
±0.50 : equal or more than 10mm from W/F edge

36D-1CCD-PKG2-3

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

Type of Through-hole Device

μPD3728DZ : CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

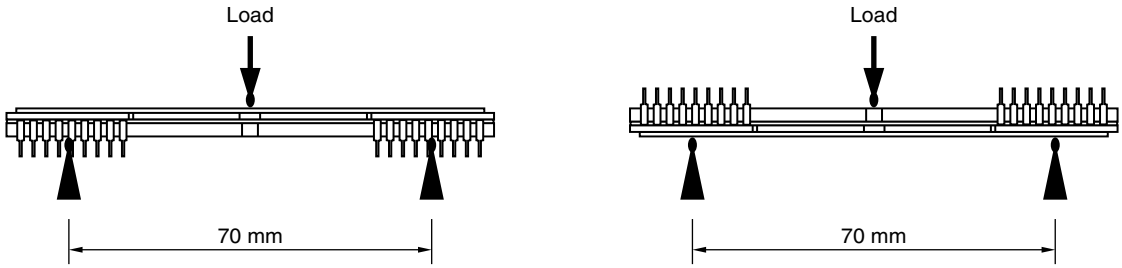
NOTES ON THE USE OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board.

For this product, the reference value for the three-point bending strength [Note] is 180 [N] (at distance between supports: 70 mm). Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body (ceramic).

Note Three-point bending strength test

Distance between supports: 70 mm, Support R: R 2 mm, Loading rate: 0.5 mm/min.



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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