

7500 PIXELS \times 3 COLOR CCD LINEAR IMAGE SENSOR**DESCRIPTION**

The μ PD3768 is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μ PD3768 has 3 rows of 7500 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 7500 pixels separately in odd and even pixels. Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers, color scanners and so on.

FEATURES

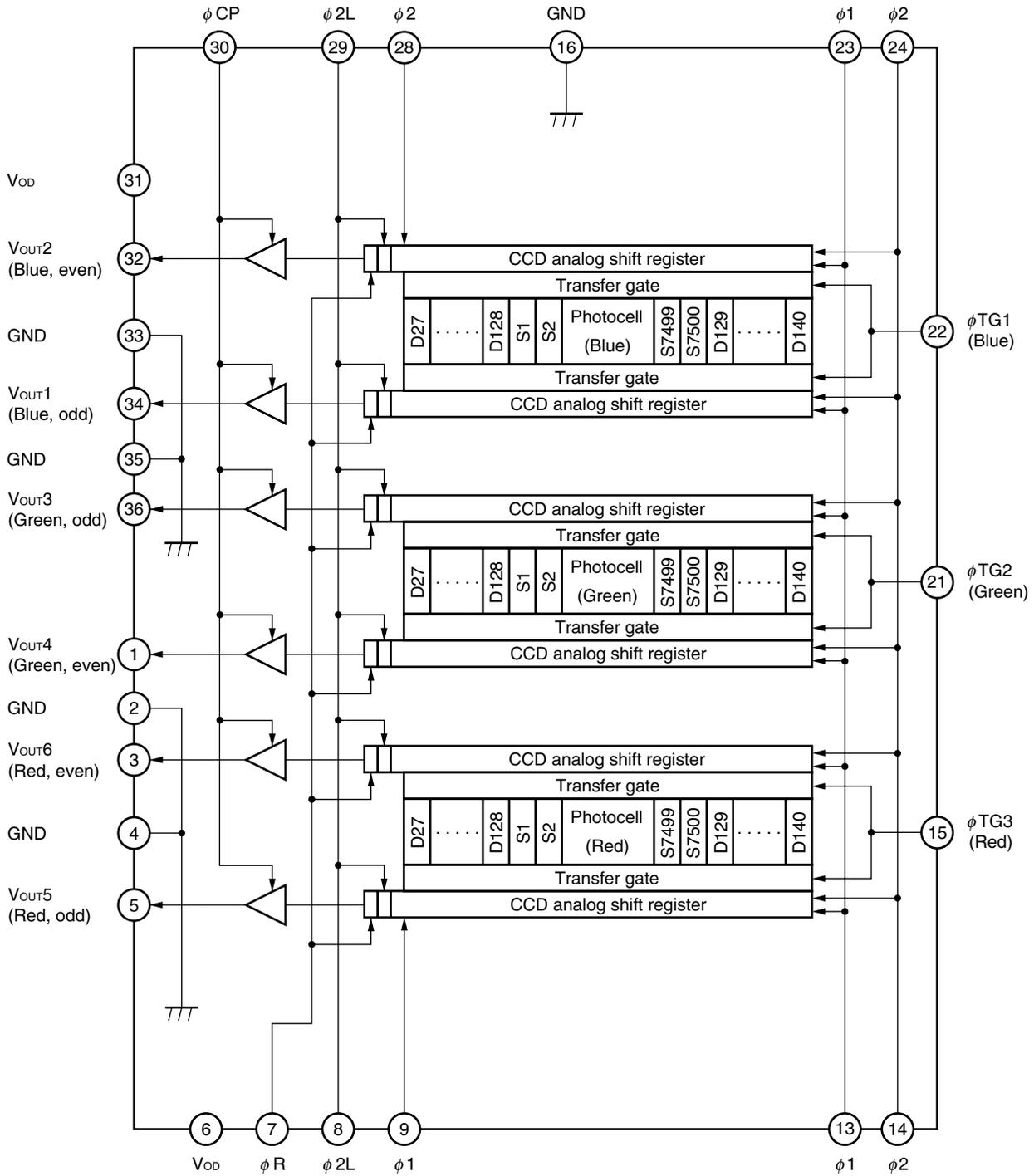
- Valid photocell : 7500 pixels \times 3
- Photocell pitch : 9.325 μ m
- Line spacing : 37.3 μ m (4 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx \cdot hour)
- Resolution : 24 dot/mm A3 (297 \times 420 mm) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 44 MHz MAX. (22 MHz/1 output)
- Output type : 2 outputs in phase/color
- Power supply : +10 V
- On-chip circuits : Reset feed-through level clamp circuits
Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μ PD3768D	CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

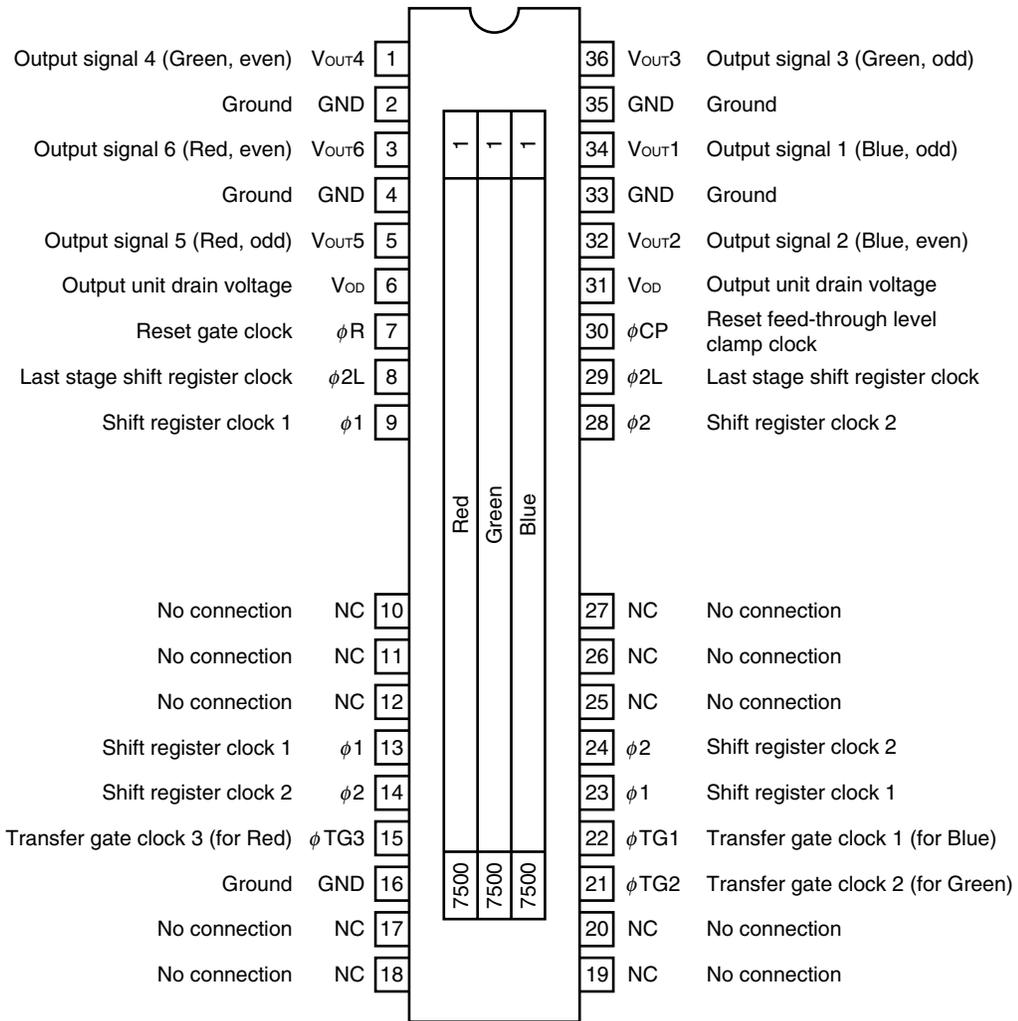
BLOCK DIAGRAM



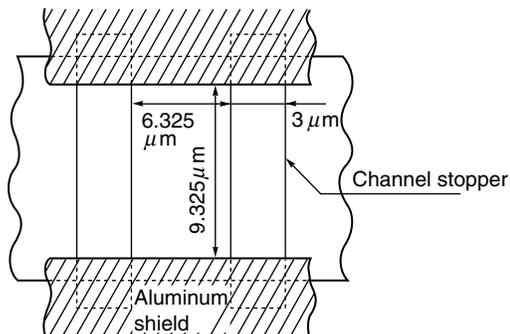
PIN CONFIGURATION (Top View)

CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

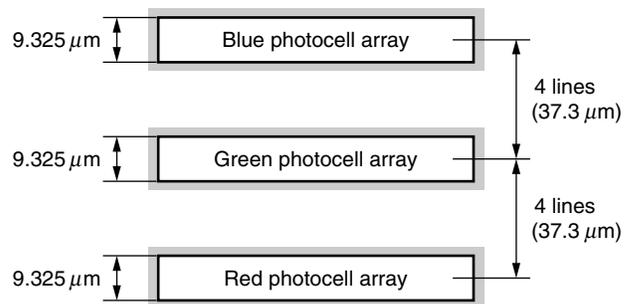
• μPD3768D



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V _{OD}	-0.3 to +12	V
Shift register clock voltage	V _{φ1} , V _{φ2}	-0.3 to +8	V
Last gate shift register clock voltage	V _{φ2L}	-0.3 to +8	V
Reset gate clock voltage	V _{φR}	-0.3 to +8	V
Clamp clock voltage	V _{φCP}	-0.3 to +8	V
Transfer gate clock voltage	V _{φTG1} to V _{φTG3}	-0.3 to +8	V
Operating ambient temperature	T _A	-25 to +60	°C
Storage temperature	T _{stg}	-40 to +100	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V _{OD}	9.5	10.0	10.5	V
Shift register clock high level	V _{φ1H} , V _{φ2H}	4.5	5.0	5.5	V
Shift register clock low level	V _{φ1L} , V _{φ2L}	-0.3	0	+0.5	V
Last gate shift register clock high level	V _{φ2LH}	4.5	5.0	5.5	V
Last gate shift register clock low level	V _{φ2LL}	-0.3	0	+0.5	V
Reset gate clock high level	V _{φRH}	4.5	5.0	5.5	V
Reset gate clock low level	V _{φRL}	-0.3	0	+0.5	V
Clamp clock high level	V _{φCPH}	4.5	5.0	5.5	V
Clamp clock low level	V _{φCPL}	-0.3	0	+0.5	V
Transfer gate clock high level	V _{φTG1H} to V _{φTG3H}	4.5	V _{φ1H} ^{Note}	V _{φ1H} ^{Note}	V
Transfer gate clock low level	V _{φTG1L} to V _{φTG3L}	-0.3	0	+0.5	V
Data rate	2f _{φR}	1	2	44	MHz

Note When Transfer gate clock high level (V_{φTG1H} to V_{φTG3H}) is higher than Shift register clock high level (V_{φ1H}), Image lag can increase.

ELECTRICAL CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$, $V_{OD} = 10\text{ V}$, $f_{\phi R} = 1\text{ MHz}$, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p} , light source (except Response1) : 2950 K halogen lamp + CM-500S (infrared cut filter, t = 1 mm))

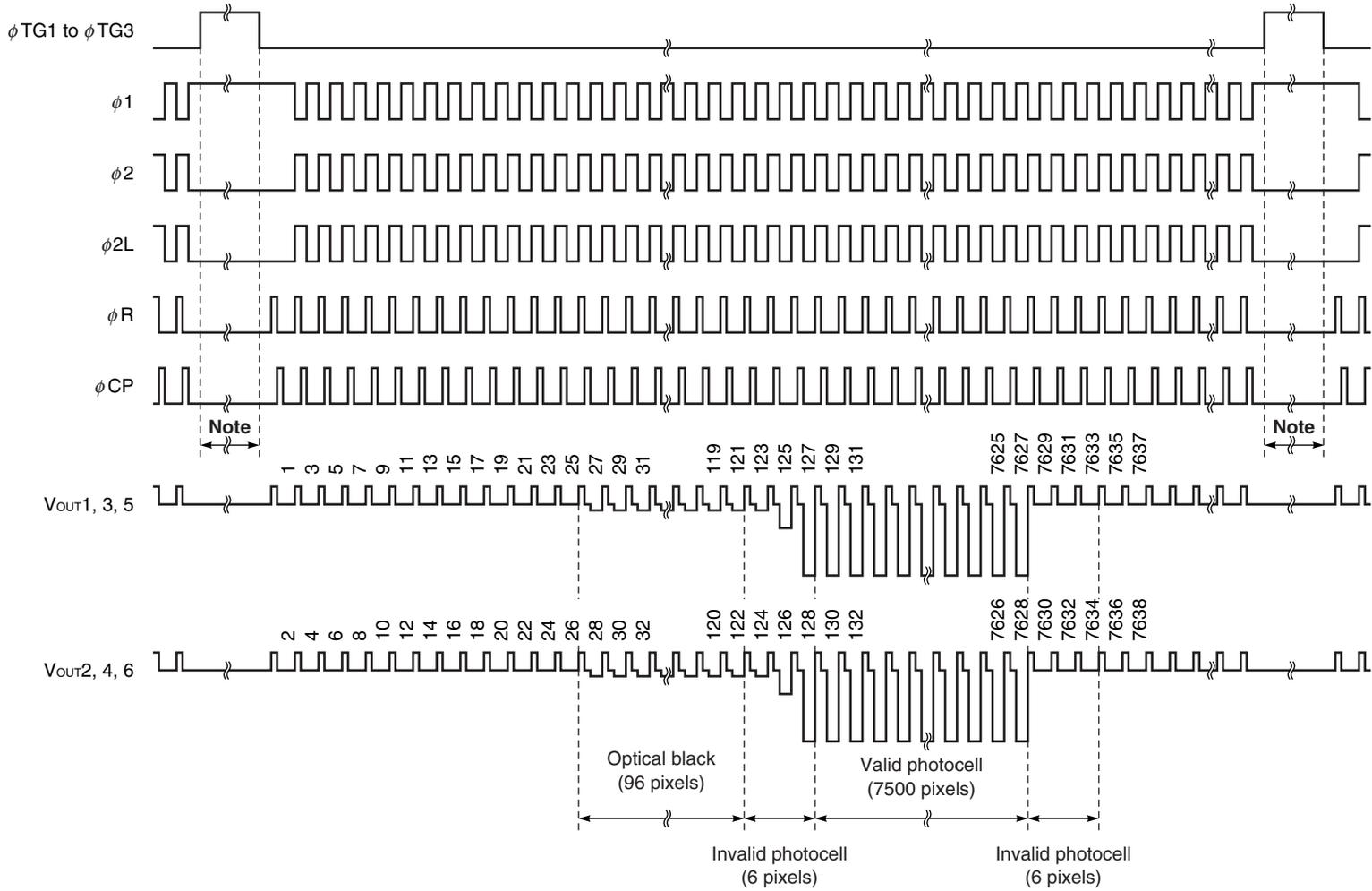
Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}		1.5	2.0	–	V
Saturation exposure	Red	SER	2950 K halogen lamp + CM-500S	–	0.14	–	lx*s
	Green	SEG		–	0.13	–	lx*s
	Blue	SEB		–	0.26	–	lx*s
Photo response non-uniformity		PRNU	$V_{OUT} = 1.0\text{ V}$	–	6.0	18.0	%
Photo response non-uniformity at low illumination		PRNU2	$V_{OUT} = 0.1\text{ V}$	–	6.0	18.0	%
Average dark signal		ADS	Light shielding, data rate = 2 MHz, storage time = 10 ms	–	1.0	5.0	mV
Dark signal non-uniformity		DSNU	Light shielding, data rate = 2 MHz, storage time = 10 ms	–	3.0	12.0	mV
Power consumption		P_w		–	700	900	mW
Output impedance		Z_o		–	0.2	0.4	kΩ
Response1	Red	R_R	3200 K halogen lamp + C-500S	15.4	22.0	28.6	V/lx*s
	Green	R_G		12.6	18.0	23.4	V/lx*s
	Blue	R_B		5.6	8.0	10.4	V/lx*s
Response2	Red	R_R	2950 K halogen lamp + CM-500S	9.8	14.0	18.2	V/lx*s
	Green	R_G		10.7	15.3	19.9	V/lx*s
	Blue	R_B		5.3	7.6	9.9	V/lx*s
Image lag		IL	$V_{OUT} = 500\text{ mV}$	–	40	80	mV
Image lag color difference		IL-DIF	$V_{OUT} = 500\text{ mV}$	–	5	20	mV
Image lag O/E		IL-O/E	$V_{OUT} = 500\text{ mV}$	–	10	30	mV
Offset level		V_{OS}		3.8	4.5	5.2	V
Output fall delay time ^{Note}		t_d		–	14	–	ns
Register imbalance		RI	$V_{OUT} = 1.0\text{ V}$	–	0	5	%
Total transfer efficiency		TTE	$V_{OUT} = 1.0\text{ V}$, $f_{\phi R} = 22\text{ MHz}$	94	98	–	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	445	–	nm
Dynamic range	DR1	$V_{sat}/DSNU$		–	666	–	times
	DR2	V_{sat}/σ_{dark}		–	870	–	times
Reset feed-through noise		RFTN	Light shielding	–1000	–200	+500	mV
Light shielding random noise		σ_{dark}	Bit clamp, $t_{17} = 10\text{ ns}$	–	2.3	–	mV

Note t_d is defined as periods from 10% of ϕ_{2L} to 10% of V_{OUT1} to V_{OUT6} (refer to **APPLICATION CIRCUIT EXAMPLE**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 10 V)

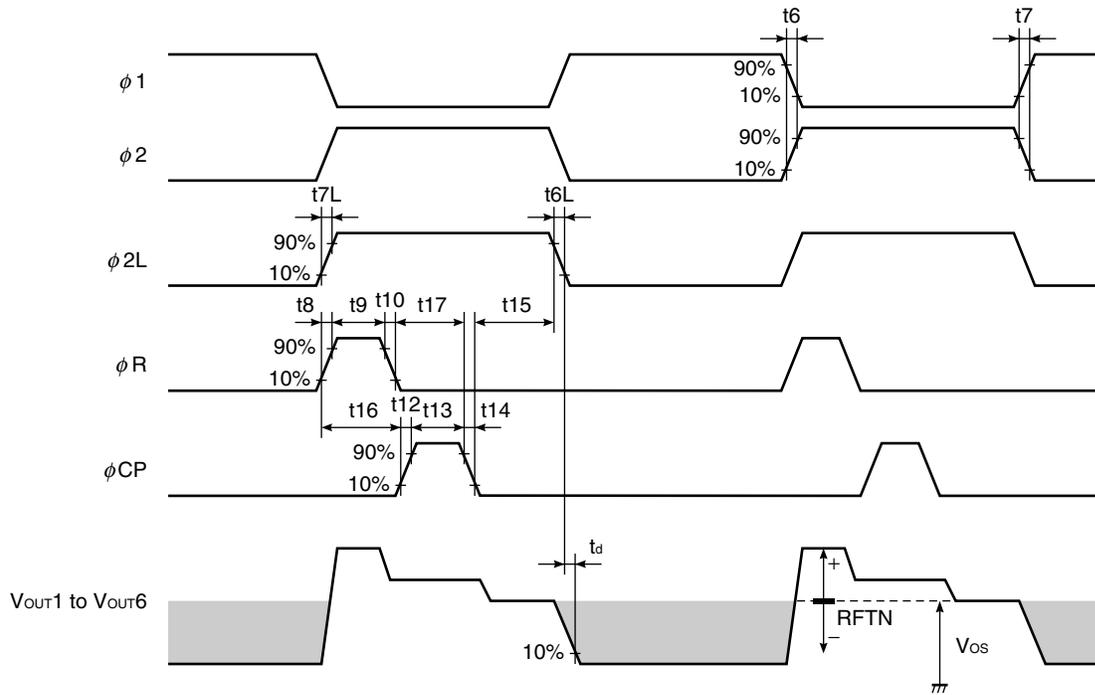
Parameter	Symbol	Pin	Pin No.	Min.	Typ.	Max.	Unit	
Shift register clock pin capacitance	C _{φ1}	φ 1	9	–	330	450	pF	
			13	–	330	450	pF	
			23	–	330	450	pF	
	C _{φ2}	φ 2	14	–	330	450	pF	
			24	–	330	450	pF	
			28	–	330	450	pF	
Last stage shift register clock pin capacitance	C _{φL}	φ 2L	8	–	10	20	pF	
			29	–	10	20	pF	
Reset gate clock pin capacitance	C _{φR}	φ R	7	–	10	20	pF	
Clamp clock pin capacitance	C _{φCP}	φ CP	30	–	10	20	pF	
Transfer gate clock pin capacitance	C _{φTG}	φ TG1	22	–	100	150	pF	
			φ TG2	21	–	100	150	pF
			φ TG3	15	–	100	150	pF

TIMING CHART 1 (Bit clamp mode, for each color)



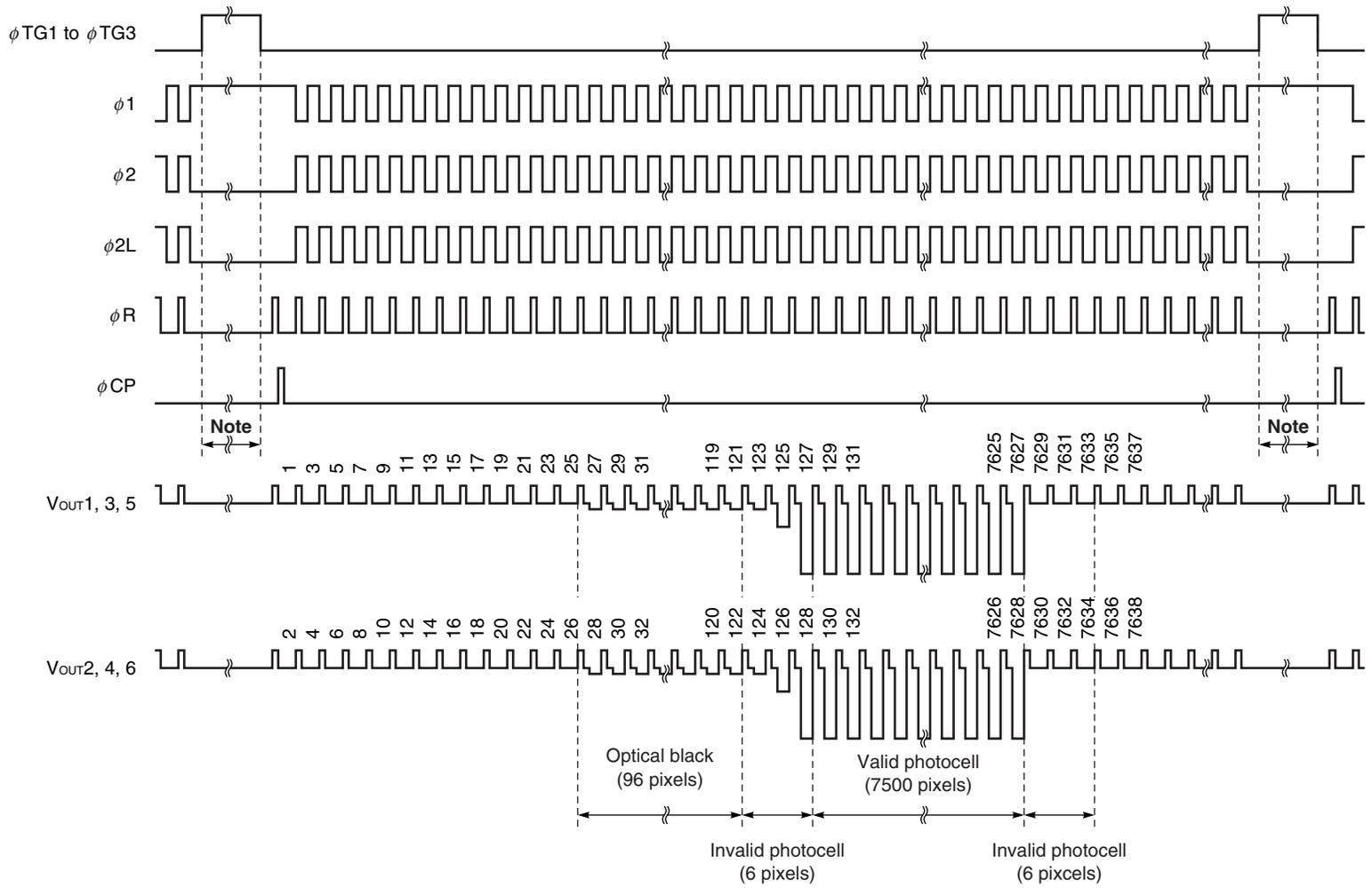
Note Set the ϕ R and ϕ CP pulse to low level during this period.

TIMING CHART 2 (Bit clamp mode, for each color)



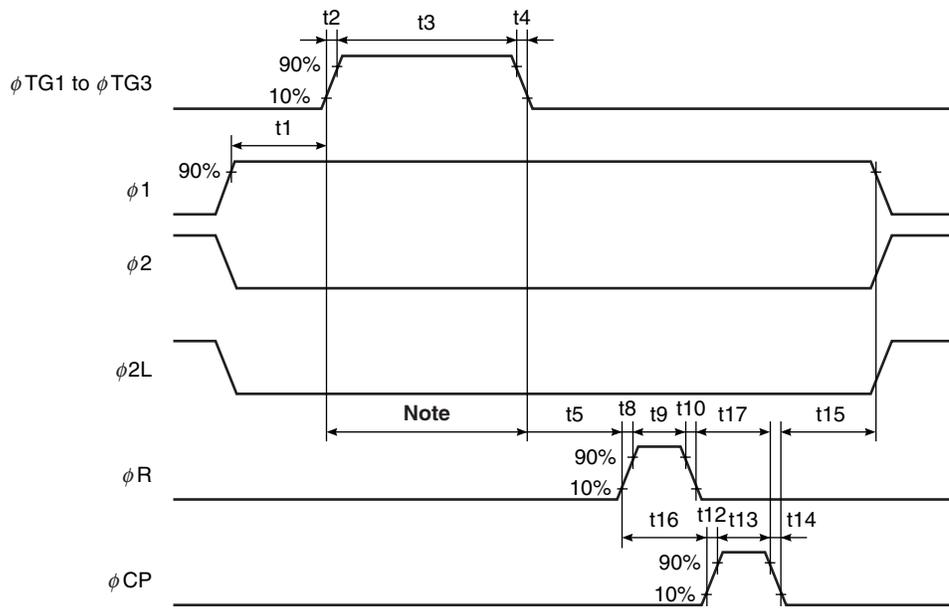
Symbol	Min.	Typ.	Max.	Unit
t6, t7	0	50	–	ns
t6L, t7L	0	5	–	ns
t8, t10	0	5	–	ns
t9	10	125	–	ns
t12, t14	0	5	–	ns
t13	10	125	–	ns
t15	0	250	–	ns
t16	8	125	–	ns
t17	8	125	–	ns

TIMING CHART 3 (Line clamp mode, for each color)



Note Set the ϕ R and ϕ CP pulse to low level during this period.

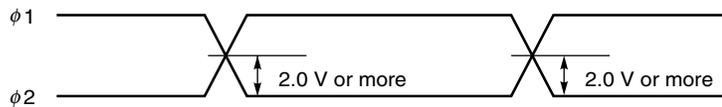
TIMING CHART 5 (Bit clamp mode, line clamp mode, for each color)



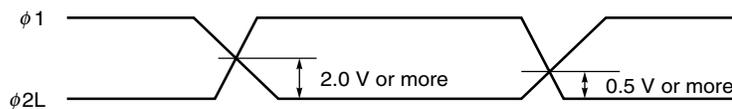
Symbol	Min.	Typ.	Max.	Unit
t1, t5	200	300	–	ns
t2, t4	0	50	–	ns
t3	3000	5000	–	ns
t8, t10	0	5	–	ns
t9	10	125	–	ns
t12, t14	0	5	–	ns
t13	10	125	–	ns
t15	0	250	–	ns
t16	8	125	–	ns
t17	8	125	–	ns

Note Set the ϕ R and ϕ CP pulse to low level during this period.

ϕ 1, ϕ 2 cross points



ϕ 1, ϕ 2L cross points



Remark Adjust cross points (ϕ 1, ϕ 2) and (ϕ 1, ϕ 2L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

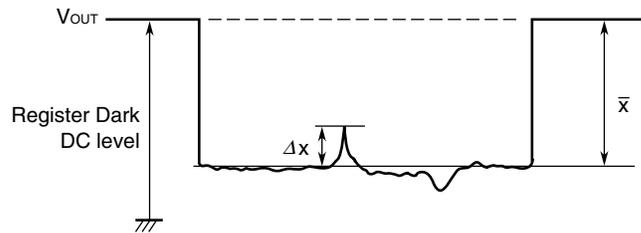
3. Photo response non-uniformity : **PRNU**
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula, and it is defined by each six of them.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

Δx : maximum of $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{7500} x_j}{7500}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

$$ADS (mV) = \frac{\sum_{j=1}^{7500} d_j}{7500}$$

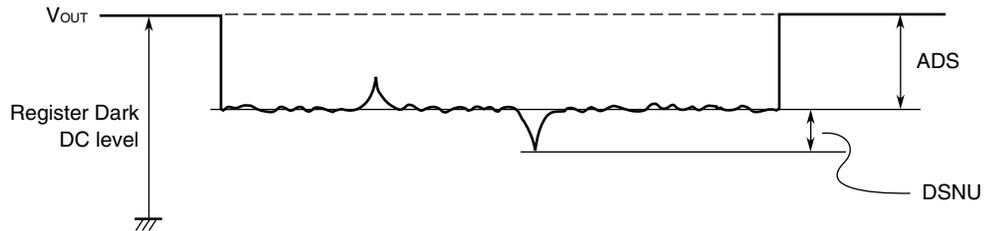
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each six of them.

$$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}|_{j=1 \text{ to } 7500}$$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

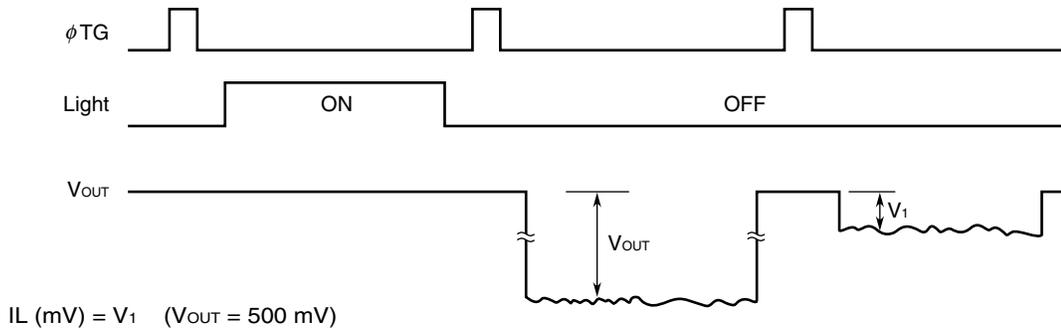
7. Response : **R**

Output voltage divided by exposure ($I \times s$).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



9. Image lag color difference : **IL-DIF**

It is defined as a difference between colors of the average of image lag.

It is expressed with the next expression to be concrete.

$$\begin{aligned} &| \text{(average of image lag of blue output)} - \text{(average of image lag of green output)} | \\ &| \text{(average of image lag of green output)} - \text{(average of image lag of red output)} | \\ &| \text{(average of image lag of red output)} - \text{(average of image lag of blue output)} | \end{aligned}$$

10. Image lag O/E : **IL-O/E**

It is defined as a difference of the average of image lag of odd and even pixels for each color.

11. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

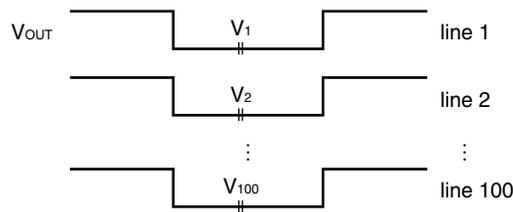
n : Number of valid pixels
 V_j : Output voltage of each pixel

12. Light shielding random noise : **σ_{dark}**

Light shielding random noise σ_{dark} is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

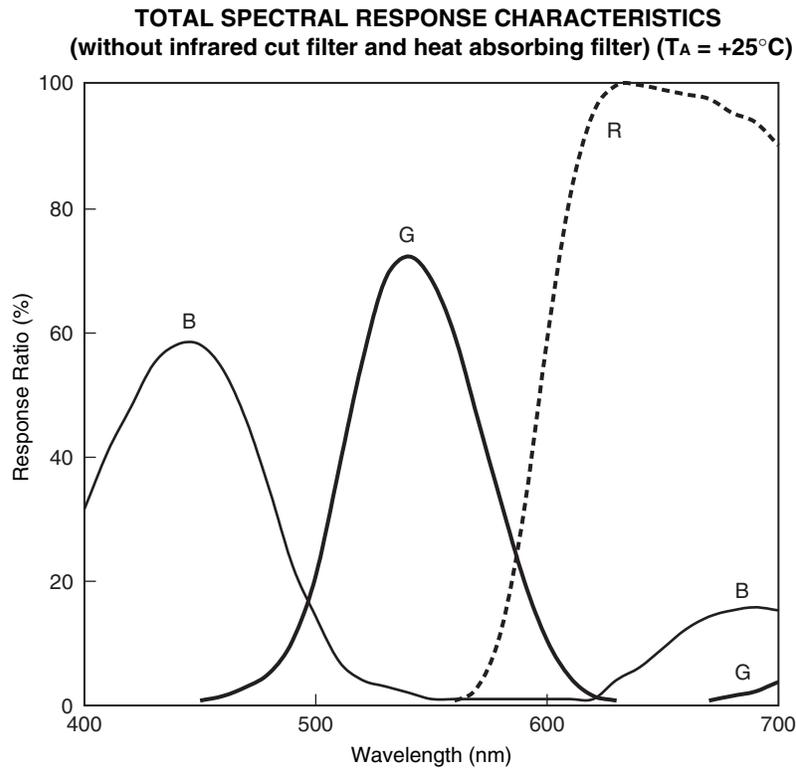
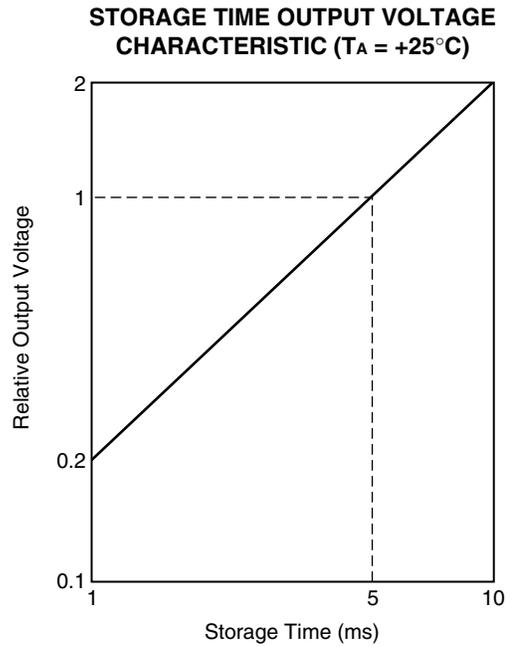
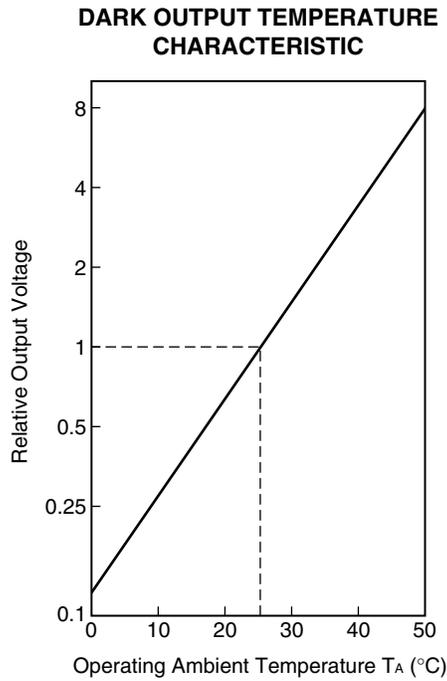
$$\sigma_{\text{dark}} (\text{mV}) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V_i : A valid pixel output signal among all of the valid pixels for each color

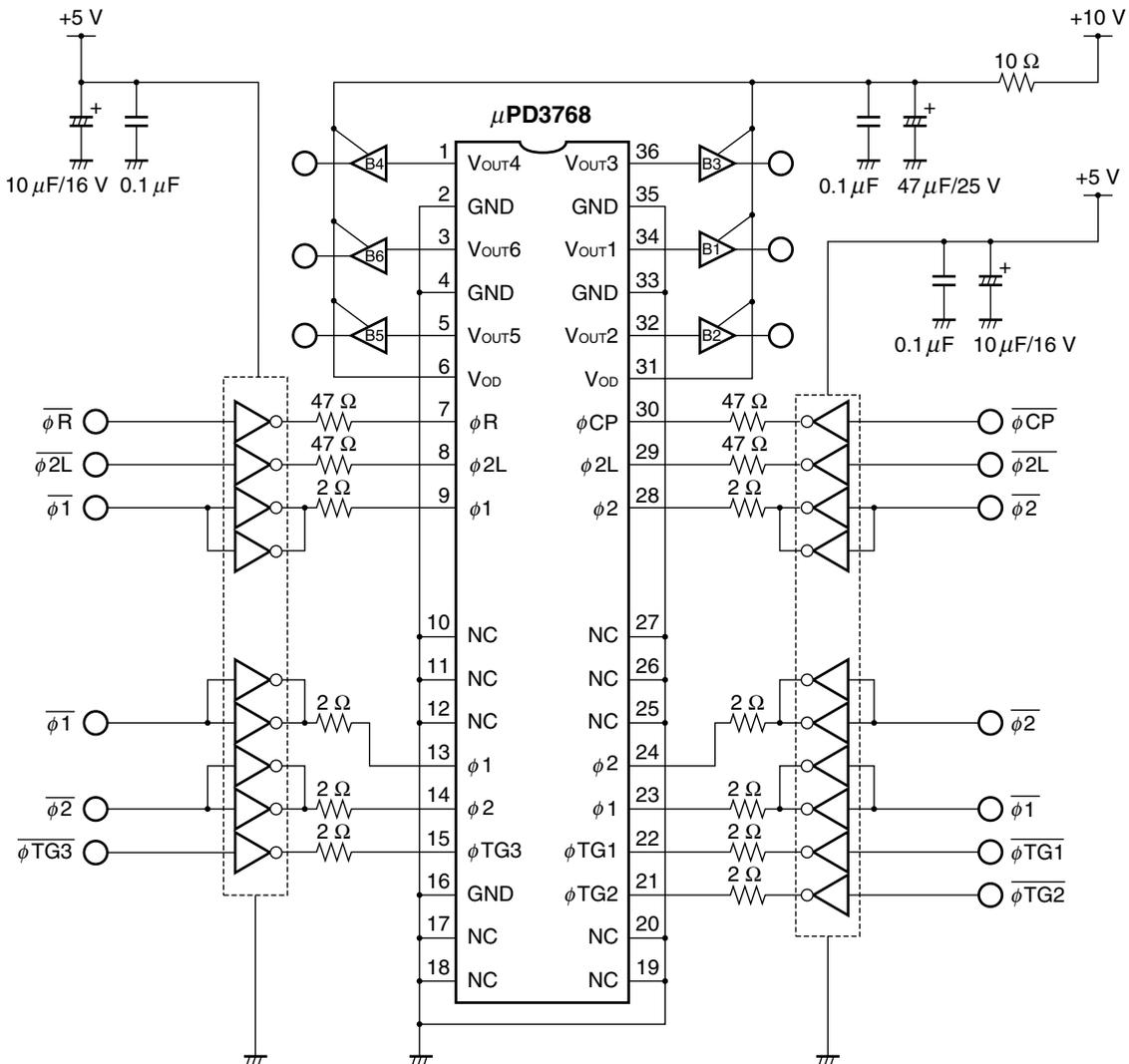


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

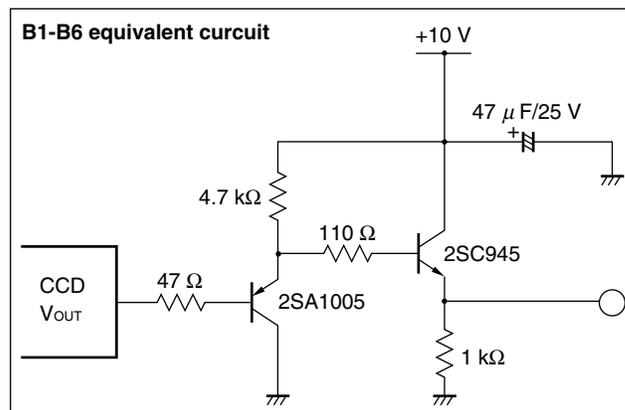
STANDARD CHARACTERISTIC CURVES (Nominal)



APPLICATION CIRCUIT EXAMPLE



- Remarks 1.** Connect two inverters (74AC04) to each $\phi 1$, $\phi 2$ pin.
- 2.** Inverters shown in the above application circuit example are the 74AC04.
- 3.** B1 to B6 in the application circuit example are shown in the figure below.



RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document “Semiconductor Device Mounting Technology Manual” (C10535E).

Type of Through-hole Device

μPD3768D : CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

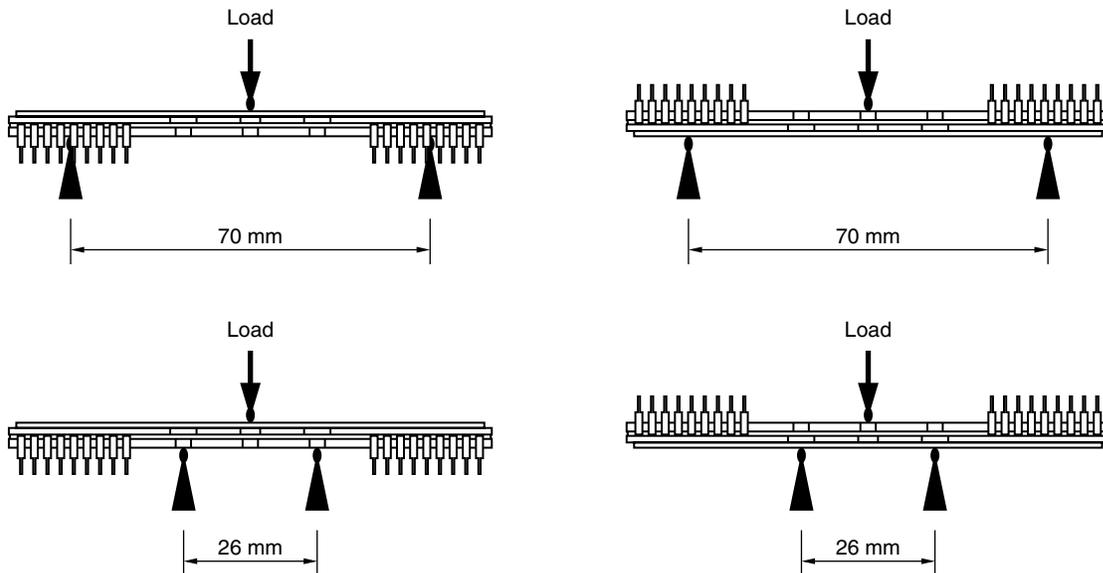
NOTES ON THE USE OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board.

For this product, the reference value for the three-point bending strength^{Note} is 180 [N] (at distance between supports: 70 mm), is 500 [N] (at distance between supports: 26 mm). Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body (ceramic).

Note Three-point bending strength test

Distance between supports: 70 mm or 26 mm, Support R: R 2 mm, Loading rate: 0.5 mm/min.



NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of May, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
 - No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
 - NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
 - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
 - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
 - NEC semiconductor products are classified into the following three quality grades:
 - "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
 - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

(Note)

- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
- (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).