

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

CCD 图像传感器

 μ PD37975300 PIXELS $\times$ 3 COLOR CCD LINEAR IMAGE SENSOR

The μ PD3797 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μ PD3797 has 3 rows of 5300 pixels, and each row has a single-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits, sample and hold circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

- Valid photocell : 5300 pixels $\times$ 3
- Photocell's pitch : 7 μ m
- Line spacing : 28 μ m (4 lines) Red line-Green line, Green line-Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx-hour)
- Resolution : 24 dot/mm A4 (210 $\times$ 297 mm) size (shorter side)
600 dpi US letter (8.5" $\times$ 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 5 MHz MAX.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
Sample and hold circuits
Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μ PD3797D	CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)

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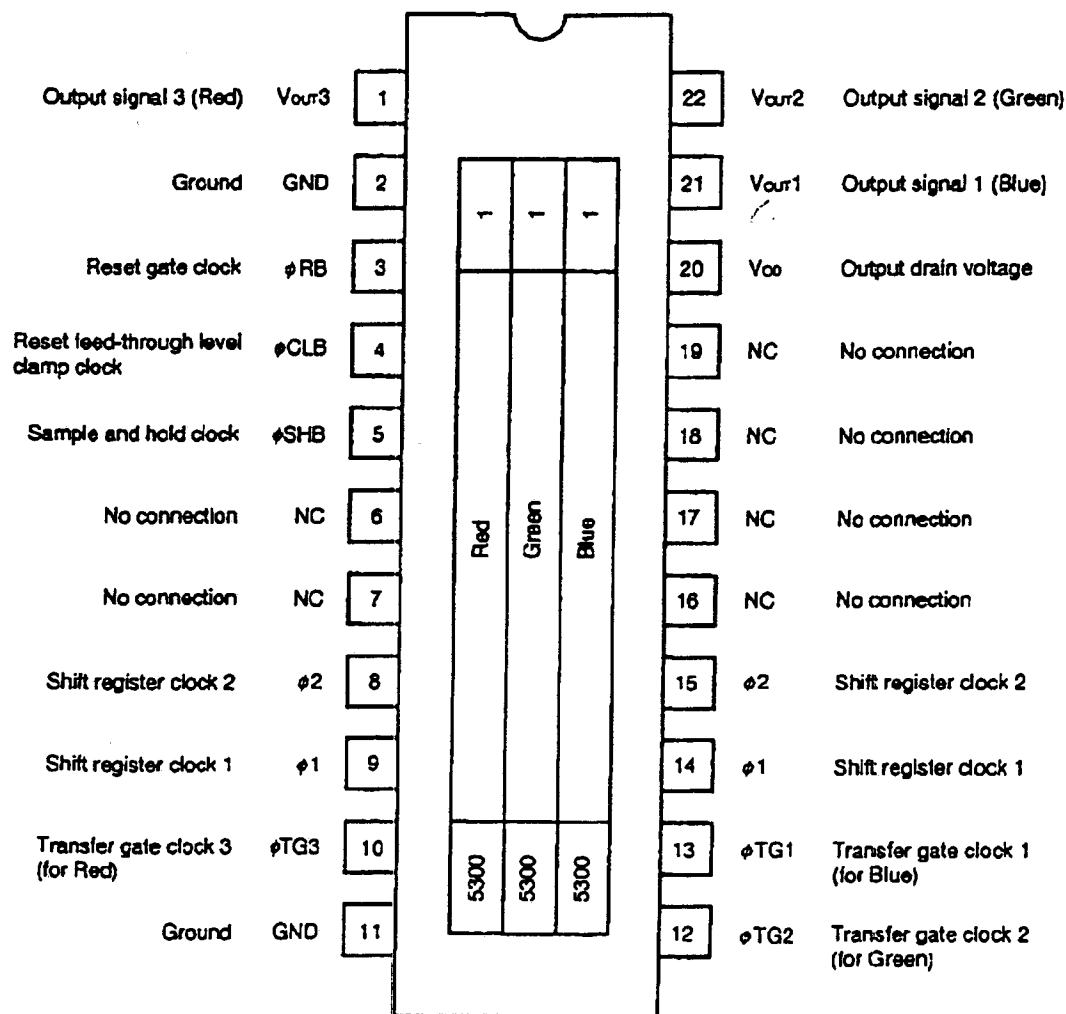
地址(Add):深圳福田区福华路福庆街鸿图大厦1602室
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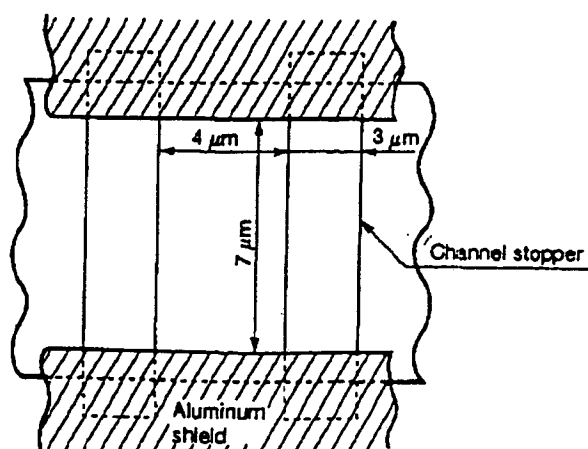
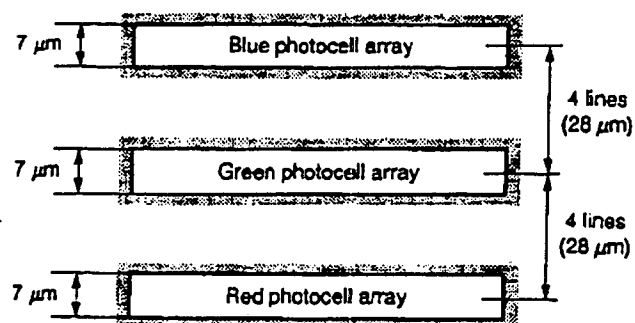
The information in this document is subject to change without notice.

PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)



PHOTOCELL STRUCTURE DIAGRAM

PHOTOCELL ARRAY STRUCTURE DIAGRAM
(Line spacing)

ABSOLUTE MAXIMUM RATINGS ($T_A = +25\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	-0.3 to +15	V
Shift register clock voltage	V_{S1}, V_{S2}	-0.3 to +15	V
Reset gate clock voltage	V_{R1B}	-0.3 to +15	V
Sample and hold clock voltage	V_{S4B4B}	-0.3 to +15	V
Reset feed-through level clamp clock voltage	V_{RCLB}	-0.3 to +15	V
Transfer gate clock voltage	V_{T01} to V_{T03}	-0.3 to +15	V
Operating ambient temperature	T_A	-25 to +60	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-40 to +100	$^{\circ}\text{C}$

Caution Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS ($T_A = +25\text{ }^{\circ}\text{C}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	V_{S1H}, V_{S2H}	4.5	5.0	5.5	V
Shift register clock low level	V_{S1L}, V_{S2L}	-0.3	0	+0.5	V
Reset gate clock high level	V_{R1BH}	4.5	5.0	5.5	V
Reset gate clock low level	V_{R1BL}	-0.3	0	+0.5	V
Sample and hold clock high level	V_{S4BH}	4.5	5.0	5.5	V
Sample and hold clock low level	V_{S4BL}	-0.3	0	+0.5	V
Reset feed-through level clamp clock high level	V_{RCLBH}	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	V_{RCLBL}	-0.3	0	+0.5	V
Transfer gate clock high level	V_{T01H} to V_{T03H}	4.5	V_{S1H} Note	V_{S1H} Note	V
Transfer gate clock low level	V_{T01L} to V_{T03L}	-0.3	0	+0.5	V
Data rate	f_{R1B}	—	1.0	5.0	MHz

Note When Transfer gate clock high level (V_{T01H} to V_{T03H}) is higher than Shift register clock high level (V_{S1H}), Image lag can increase.

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ELECTRICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, data rate (f_{PR}) = 1 MHz, storage time = 5.5 ms,
light source: 3200 K halogen lamp +C-500S (infrared cut filter, $t = 1\text{ mm}$), Input signal clock = 5 V_{pp})

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		2.0	3.0	—	V
Saturation exposure	Red	SER		0.268		lx·s
	Green	SEG		0.294		lx·s
	Blue	SEB		0.492		lx·s
Photo response non-uniformity	PRNU	$V_{\text{out}} = 1.0\text{ V}$		6	20	%
Average dark signal	ADS	Light shielding		0.2	4.0	mV
Dark signal non-uniformity	DSNU	Light shielding		2.0	4.0	mV
Power consumption	P_T			400	700	mW
Output impedance	Z_o			0.5	1	k Ω
Response	Red	R_R	7.8	11.2	14.6	V/lx·s
	Green	R_G	7.1	10.2	13.3	V/lx·s
	Blue	R_B	4.2	6.1	8.0	V/lx·s
Image lag	IL	$V_{\text{out}} = 1.0\text{ V}$		3.0	10.0	%
Offset level ^{Note1}	V_{os}		4.0	5.5	7.0	V
Output fall delay time ^{Note2}	t_d	$V_{\text{out}} = 1.0\text{ V}$		40		ns
Total transfer efficiency	TTE	$V_{\text{out}} = 1.0\text{ V}$, data rate = 5 MHz	92	98		%
Response peak	Red			630		nm
	Green			540		nm
	Blue			460		nm
Dynamic range	DR1	$V_{\text{sat}}/\text{DSNU}$		1500		times
	DR2	V_{sat}/σ		3000		times
Reset feed-through noise ^{Note1}	RFTN	Light shielding. Non-sample and hold mode	-1000	-300	+500	mV
Random noise	σ	Light shielding	—	1.0	—	mV

Notes 1. Refer to TIMING CHART 2.

2. When the fall time of $\phi 1$ (t_1) is the TYP. value (refer to TIMING CHART 2).

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INPUT PIN CAPACITANCE ($T_A = +25\text{ }^{\circ}\text{C}$, $V_{DD} = 12\text{ V}$)

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	$\phi 1$	9		400		pF
			14		400		pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	$\phi 2$	8		400		pF
			15		400		pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	3		15		pF
Sample and hold clock pin capacitance	$C_{\phi SHB}$	ϕSHB	5		15		pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	4		15		pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	$\phi TG1$	13		100		pF
		$\phi TG2$	12		100		pF
		$\phi TG3$	10		100		pF

Remark Pins 9 and 14 ($\phi 1$), 8 and 15 ($\phi 2$) are each connected inside of the device.

SAMPLE AND HOLD FUNCTION

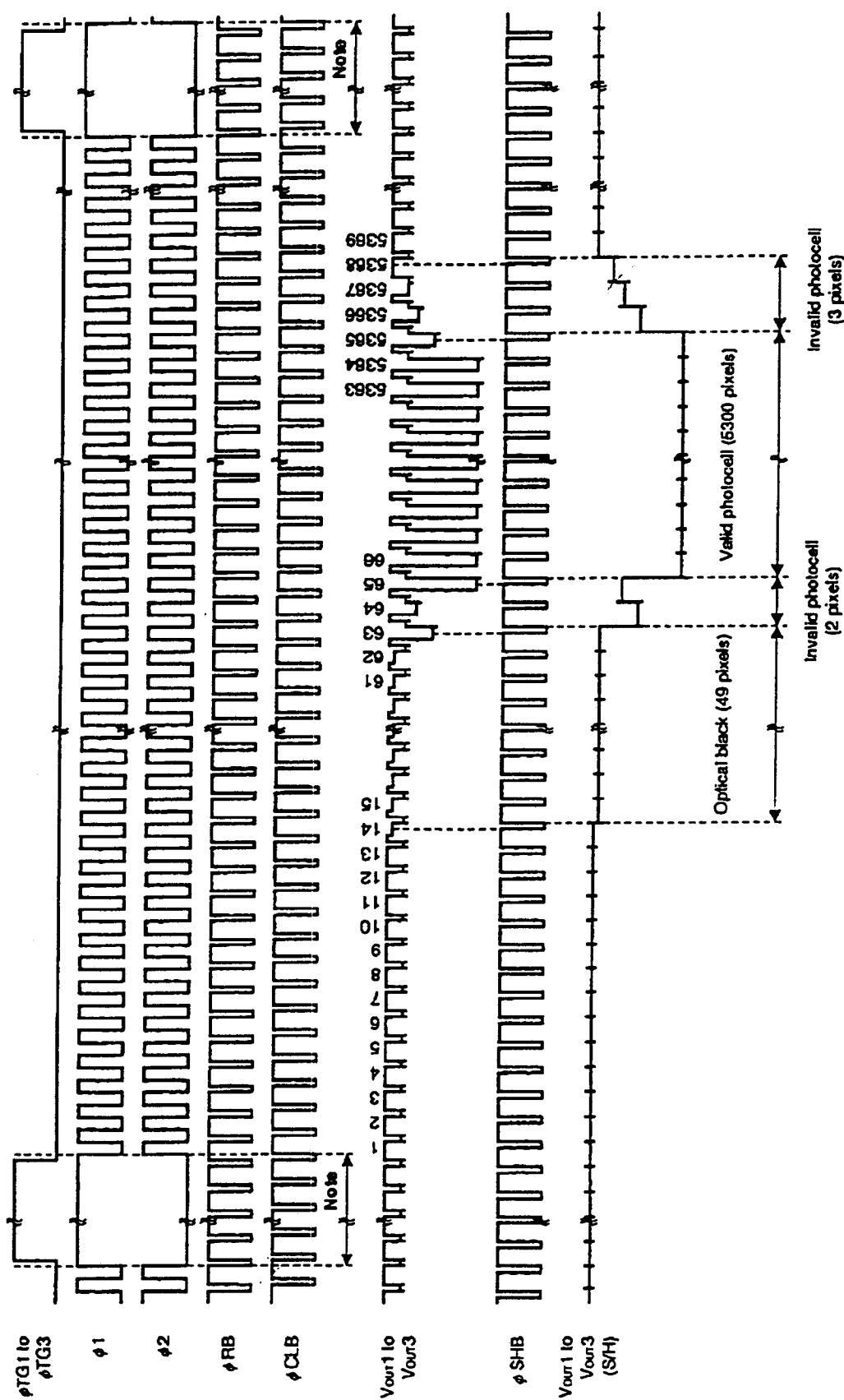
ϕSHB	Output type
Pulse	Sample and hold type
DC low level	Non-sample and hold type
DC high level	Prohibited

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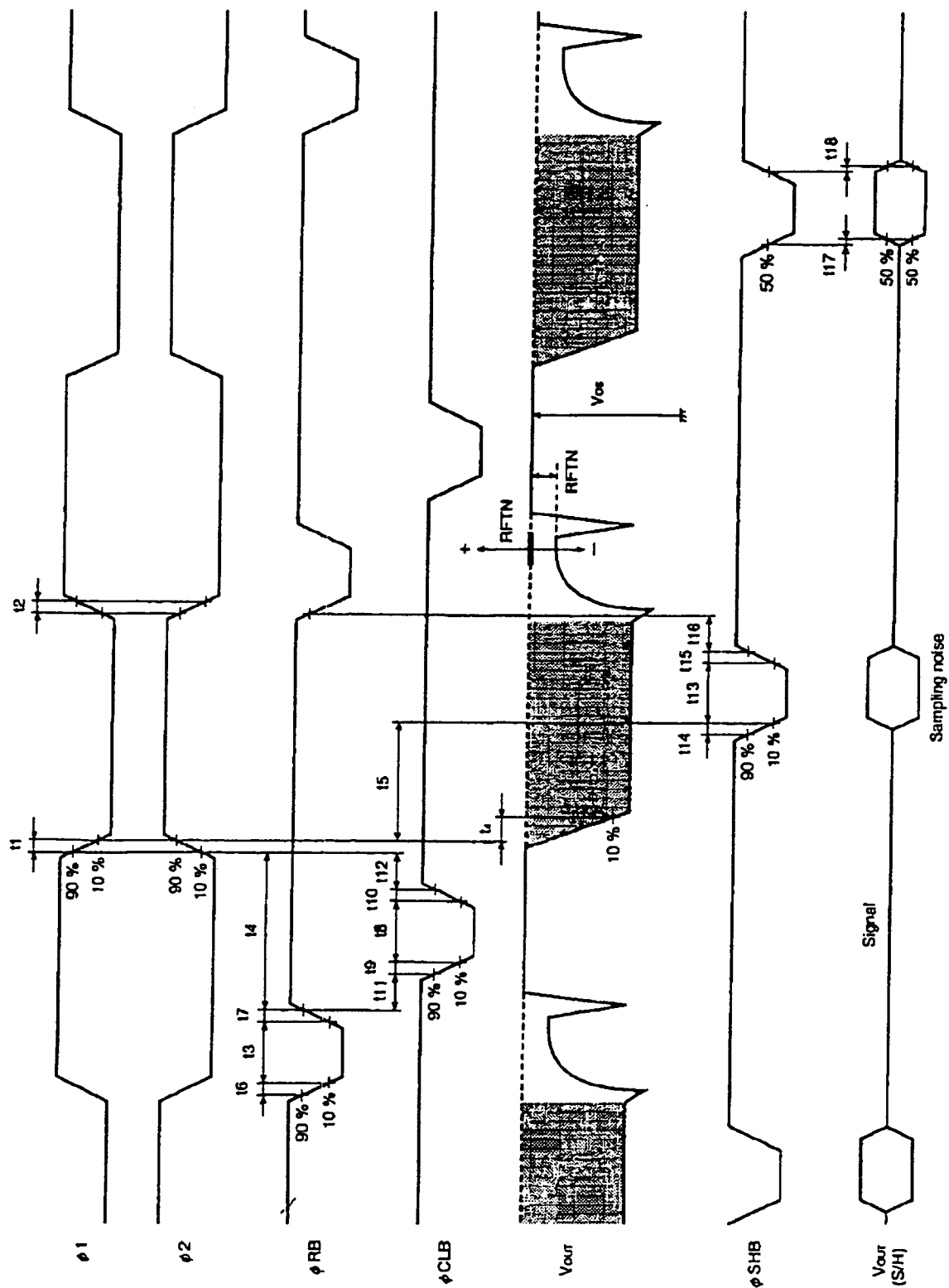
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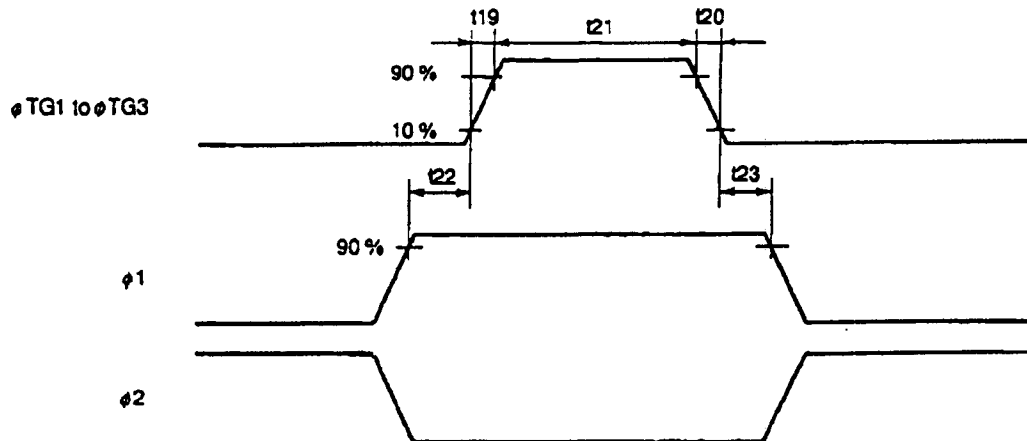
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TIMING CHART 1 (for each color)

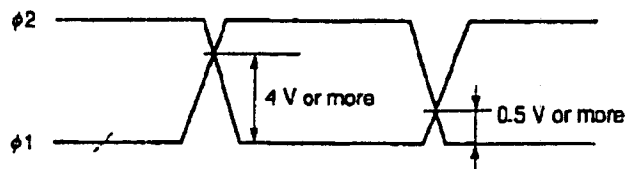


Note Input the ϕ RB and ϕ CLB pulses continuously during this period. And also input the ϕ SHB pulse when the on-chip sample and hold function is used.



ϕ TG1 to ϕ TG3, ϕ 1, ϕ 2 TIMING CHART

Symbol	MIN.	TYP.	MAX.	Unit
t_1, t_2	0	25		ns
t_3	30	60		ns
t_4	60	250		ns
t_5	60	200		ns
t_6, t_7	0	25		ns
t_8	40	100		ns
t_9, t_{10}	0	25		ns
t_{11}	10	50		ns
t_{12}	0	5		ns
t_{13}	40	150		ns
t_{14}, t_{15}	0	25		ns
t_{16}	0	30		ns
t_{17}, t_{18}	0	10	—	ns
t_{19}, t_{20}	0	50		ns
t_{21}	3000	10000		ns
t_{22}, t_{23}	900	1000		ns

 ϕ 1, ϕ 2 cross points

Remark Adjust cross points of ϕ 1 and ϕ 2 with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}

Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

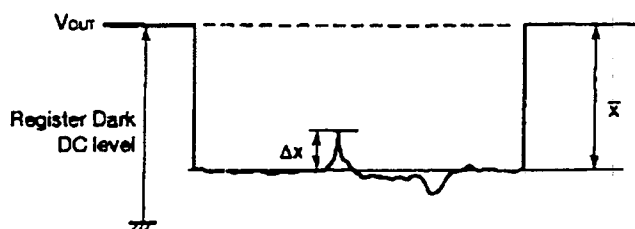
3. Photo response non-uniformity: PRNU

The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

 Δx : maximum of $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{5300} x_j}{5300}$$

 x_j : Output voltage of valid pixel number j 

4. Average dark signal: ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

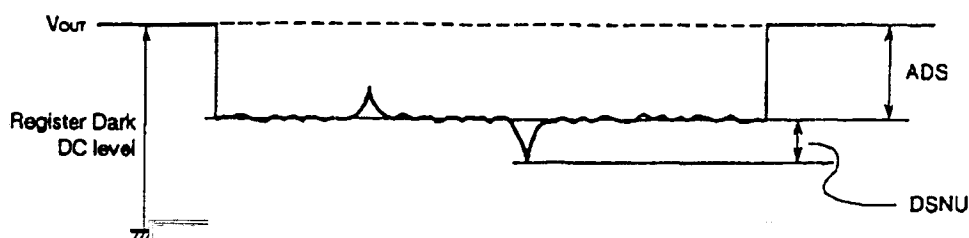
$$ADS (mV) = \frac{\sum_{j=1}^{5300} d_j}{5300}$$

 d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$DSNU (mV) : \text{maximum of } |d_j - ADS|_{j=1 \text{ to } 5300}$$

 d_j : Dark signal of valid pixel number j 

6. Output impedance: Z_o

Impedance of the output pins viewed from outside.

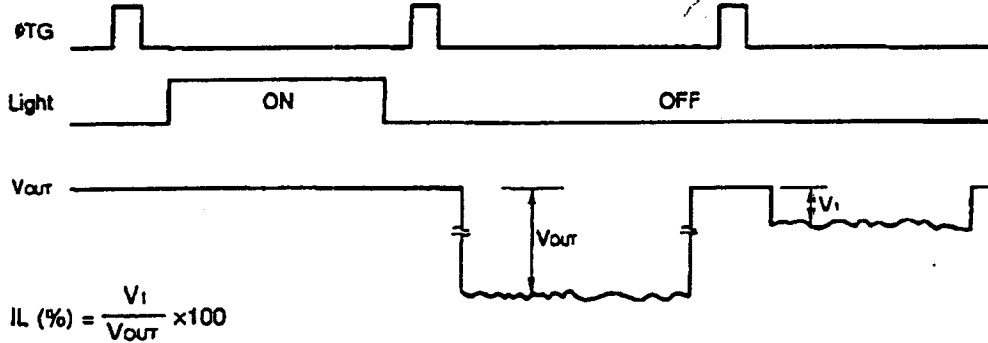
7. Response: R

Output voltage divided by exposure (lx·s).

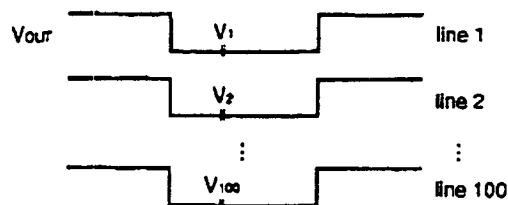
Note that the response varies with a light source (spectral characteristic).

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.

9. Random noise: σ Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding).

$$\sigma (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

 V_i : A valid pixel output signal among all of the valid pixels for each color

This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

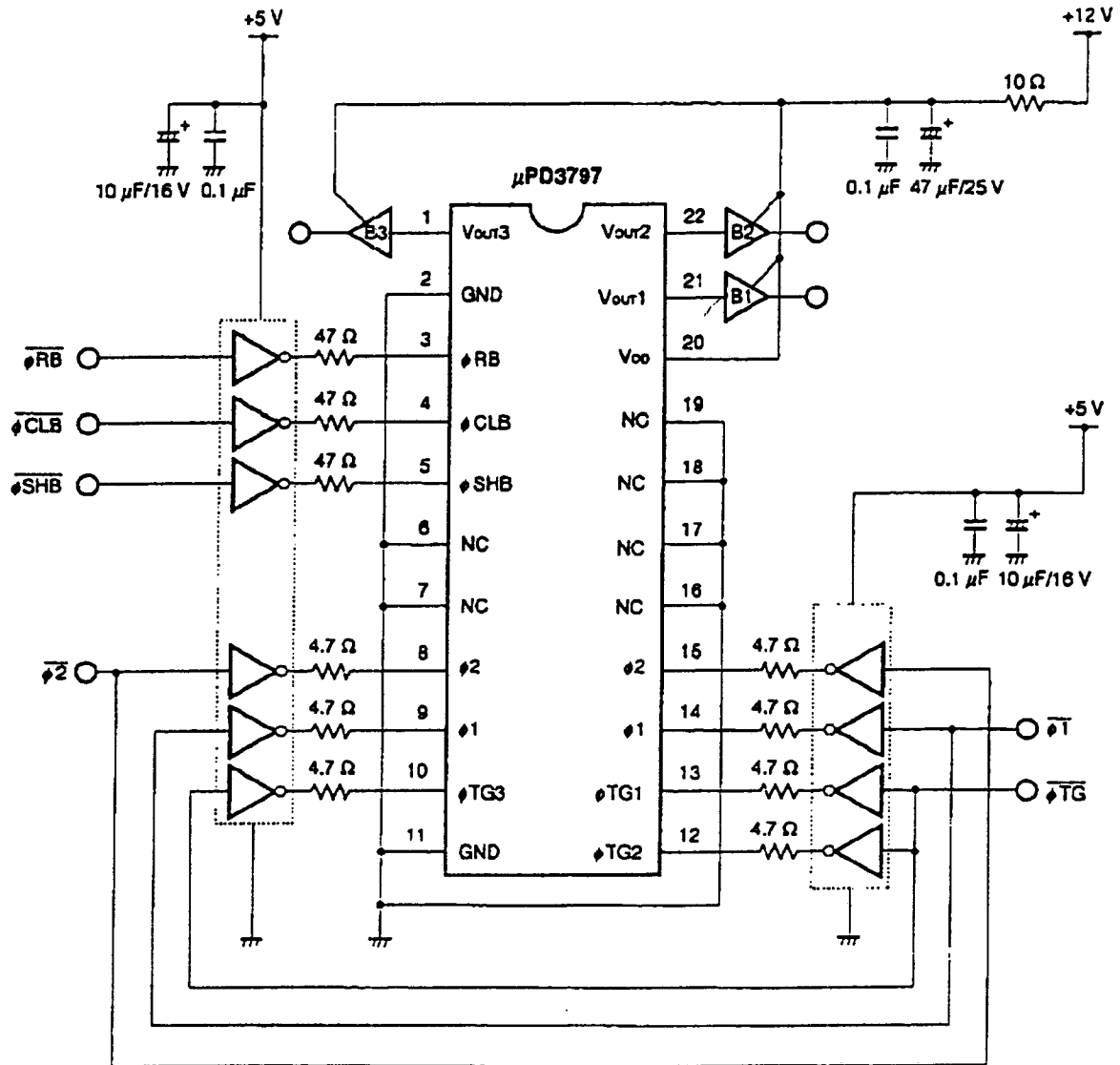
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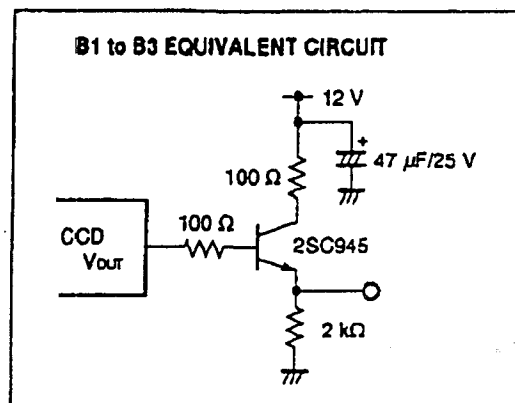
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APPLICATION CIRCUIT EXAMPLE



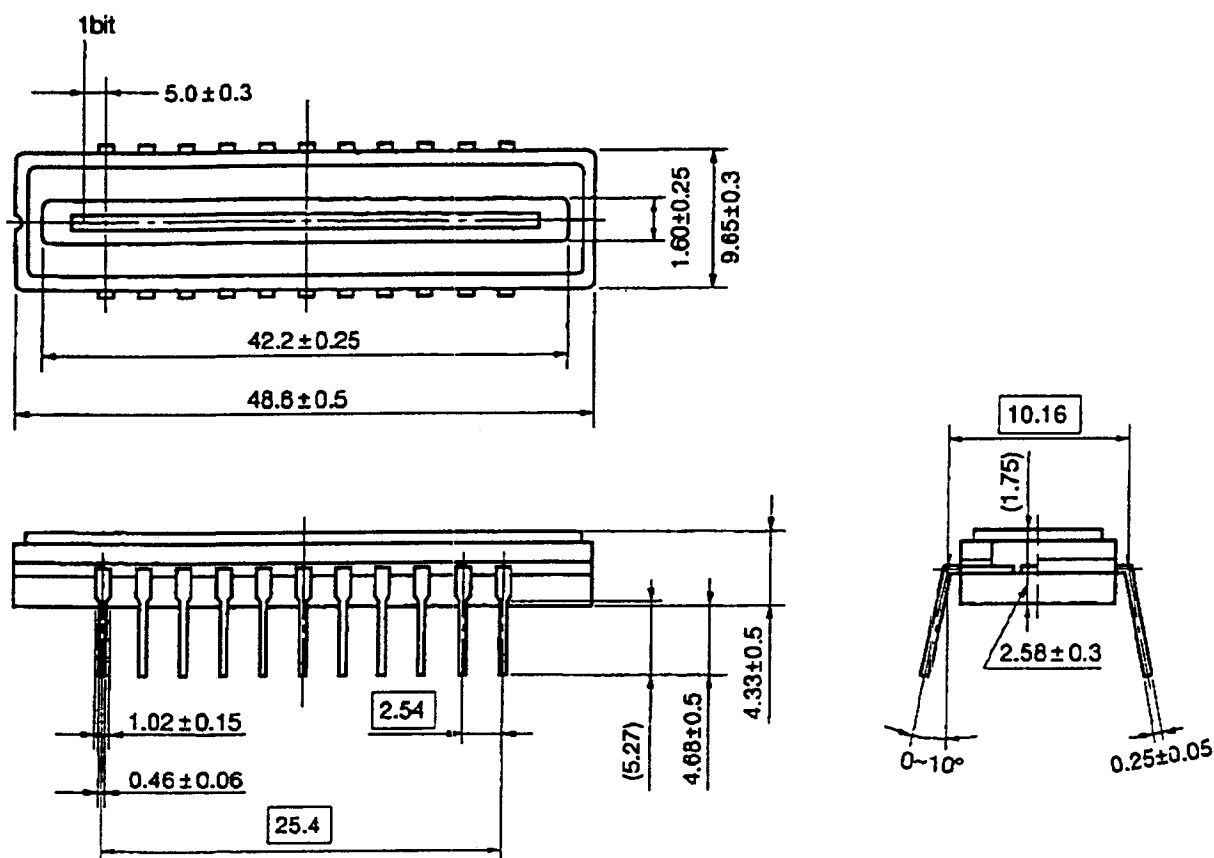
- Remarks**
1. When internal sample and hold circuit of the μ PD3797 is not necessary, connect pin 5 (ϕ SHB) to GND.
 2. The inverters shown in the above application circuit example are the 74HC04.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP(CERDIP)(400mII)

(Unit : mm)



Name	Dimensions	Refractive Index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG9

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RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "Semiconductor Device Mounting Technology Manual"(C10535E).

Type of Through-hole Device

μ PD3797D: CCD linear image sensor 22-pin ceramic DIP (CERDIP) (400 mil)

Process	Conditions
Partial heating method	Pin temperature: 260 °C or below, Heat Time: 10 seconds or less (per pin)

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

NEC

μPD3797

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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