NEC

MOS INTEGRATED CIRCUIT

μPD8871

10680 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8871 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD8871 has 3 rows of 10680 pixels, and each row has a single-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 1200 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

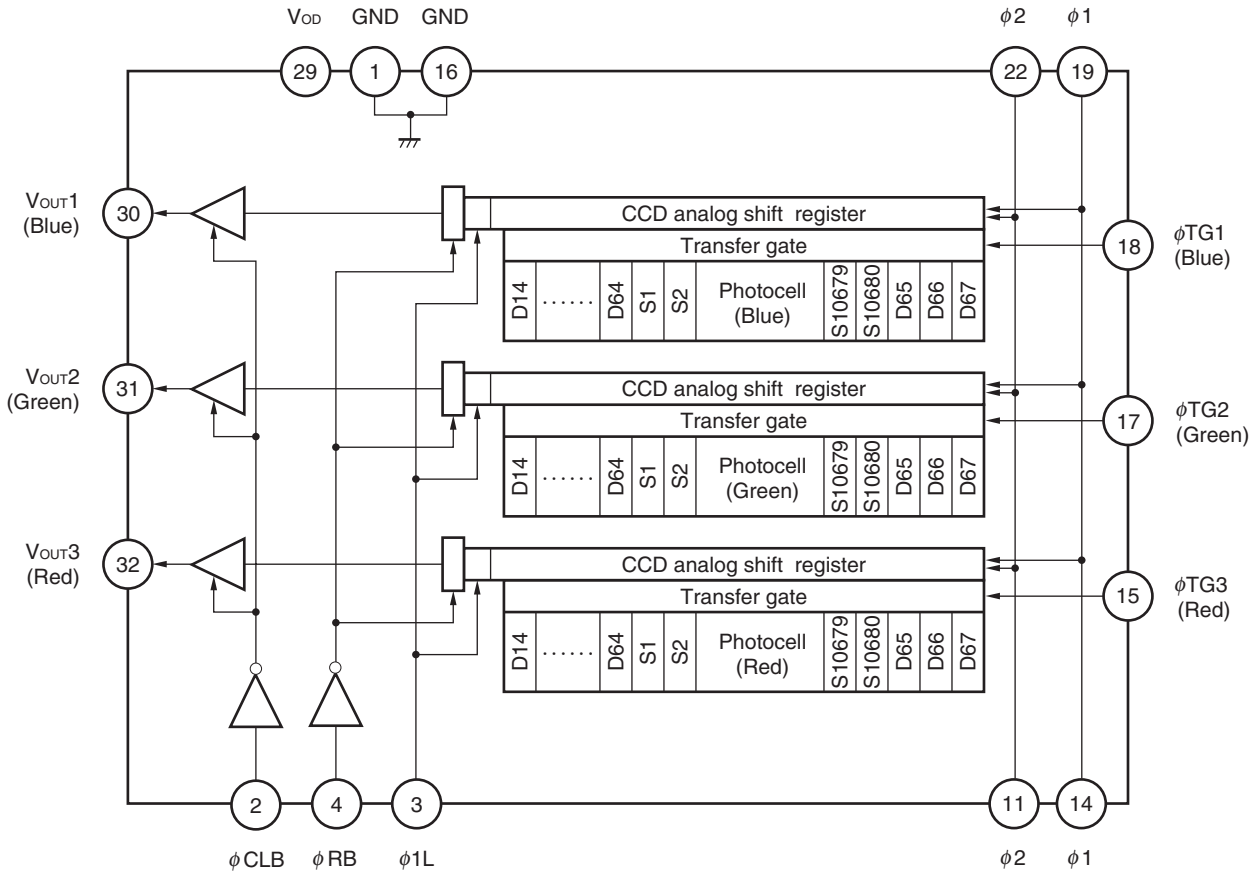
- Valid photocell : 10680 pixels × 3
- Photocell pitch : 4 μm
- Photocell size : $4 \times 4\ \mu m^2$
- Line spacing : 32 μm (8 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
- Resolution : 48 dot/mm A4 (210 × 297 mm) size (shorter side)
  1200 dpi US letter (8.5" × 11") size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 10 MHz Max.
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8871CY	CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Document No. S15329EJ1V1DS00 (1st edition)
Date Published May 2001 NS CP (K)
Printed in Japan

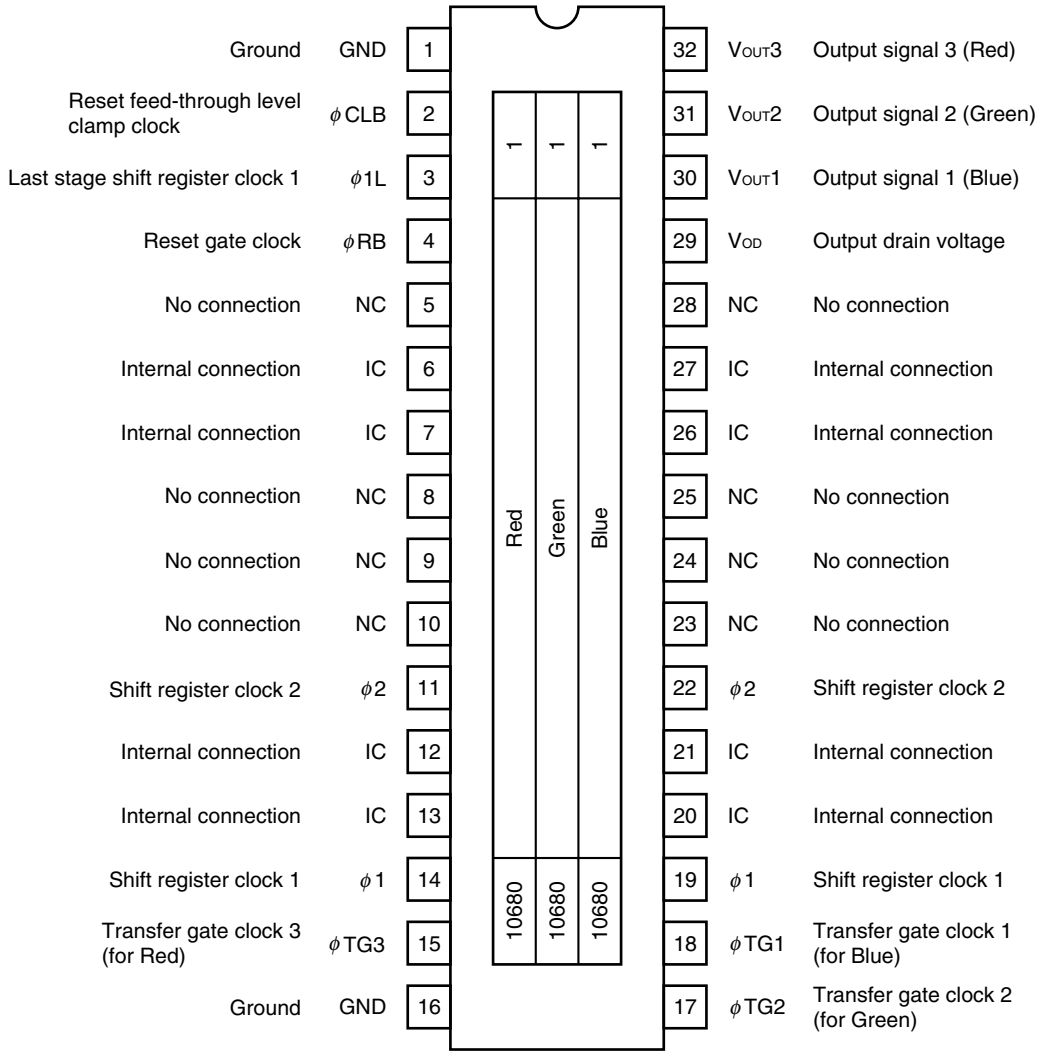
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

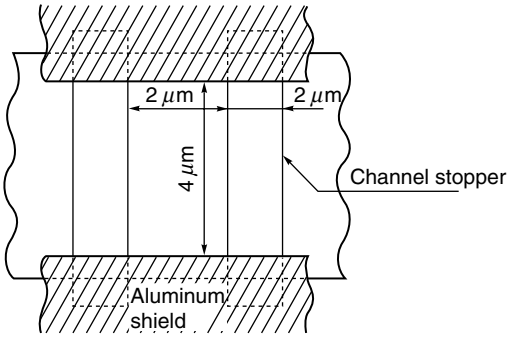
CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

• μPD8871CY

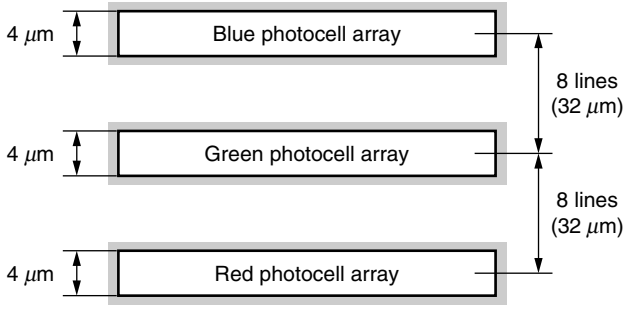


Caution Leave pins 6 , 7, 12, 13, 20, 21, 26, 27 (IC) unconnected.

PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 1L}$	−0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	−0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	−0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	−0.3 to +8	V
Operating ambient temperature	T_A	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 1LH}$	4.75	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 1LL}$	−0.3	0	+0.25	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	−0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	−0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.75	$V_{\phi 1H}$ Note	$V_{\phi 1H}$ Note	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	−0.3	0	+0.15	V
Data rate	$f_{\phi RB}$	−	2.0	10.0	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than Shift register clock high level ($V_{\phi 1H}$), Image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 2 MHz, storage time = 5.5 ms, input signal clock = 5 V_{p-p}, light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}		2.5	3.2	–	V
Saturation exposure	Red	SER		–	0.889	–	lx•s
	Green	SEG		–	0.970	–	lx•s
	Blue	SEB		–	1.455	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6	20	%
Average dark signal		ADS	Light shielding	–	0.2	4.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	1.0	4.0	mV
Power consumption		P_W		–	360	540	mW
Output impedance		Z_O		–	0.30	1.00	kΩ
Response	Red	R_R		2.52	3.60	4.68	V/lx•s
	Green	R_G		2.31	3.30	4.29	V/lx•s
	Blue	R_B		1.54	2.20	2.86	V/lx•s
Image lag		IL	V_{OUT} = 1.0 V	–	1.0	7.0	%
Offset level Note 1		V_{OS}		4.5	6.0	7.5	V
Output fall delay time Note 2		t_d	V_{OUT} = 1.0 V, (t1') = 5 ns	–	25	–	ns
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 10 MHz	92	98	–	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	460	–	nm
Dynamic range		DR1	V_{sat}/DSNU	–	3200	–	times
		DR2	V_{sat}/σCDS	–	3200	–	times
Reset feed-through noise Note 1		RFTN	Light shielding	–2000	+100	+1000	mV
Random noise (CDS)		σCDS	Light shielding	–	1.0	–	mV

Notes 1. Refer to **TIMING CHART 2, 3**.

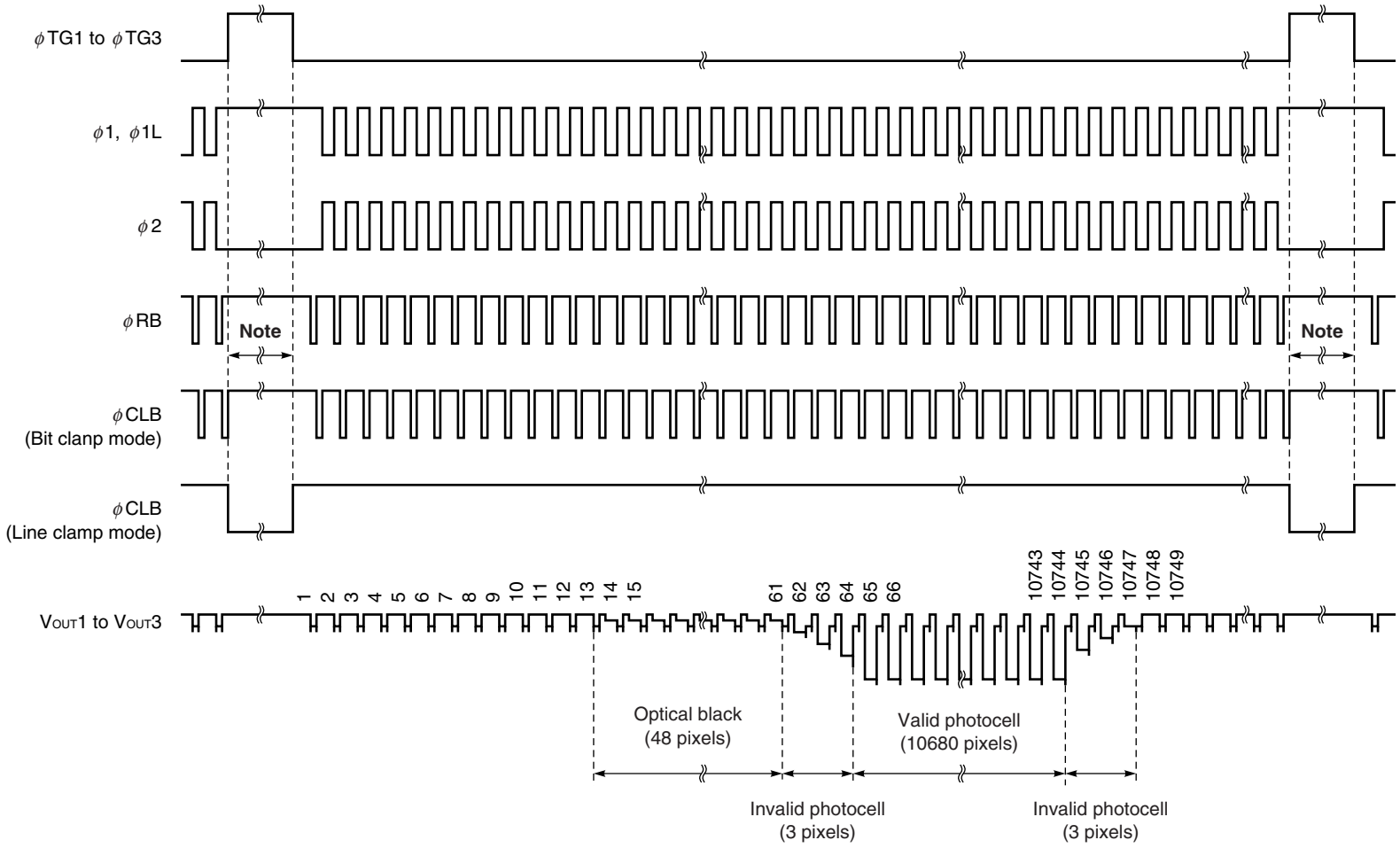
2. When the fall time of ϕ1L (t1') is the Typ. value (refer to **TIMING CHART 2, 3**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$	ϕ1	14	–	450	–	pF
			19	–	450	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$	ϕ2	11	–	450	–	pF
			22	–	450	–	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ1L	3	–	10	–	pF
Reset gate clock pin capacitance	$C_{\phi RB}$	ϕRB	4	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	ϕCLB	2	–	10	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG1	18	–	100	–	pF
		ϕTG2	17	–	100	–	pF
		ϕTG3	15	–	100	–	pF

Remark Pin 14 and 19 (ϕ1), 11 and 22 (ϕ2) are each connected inside of the device.

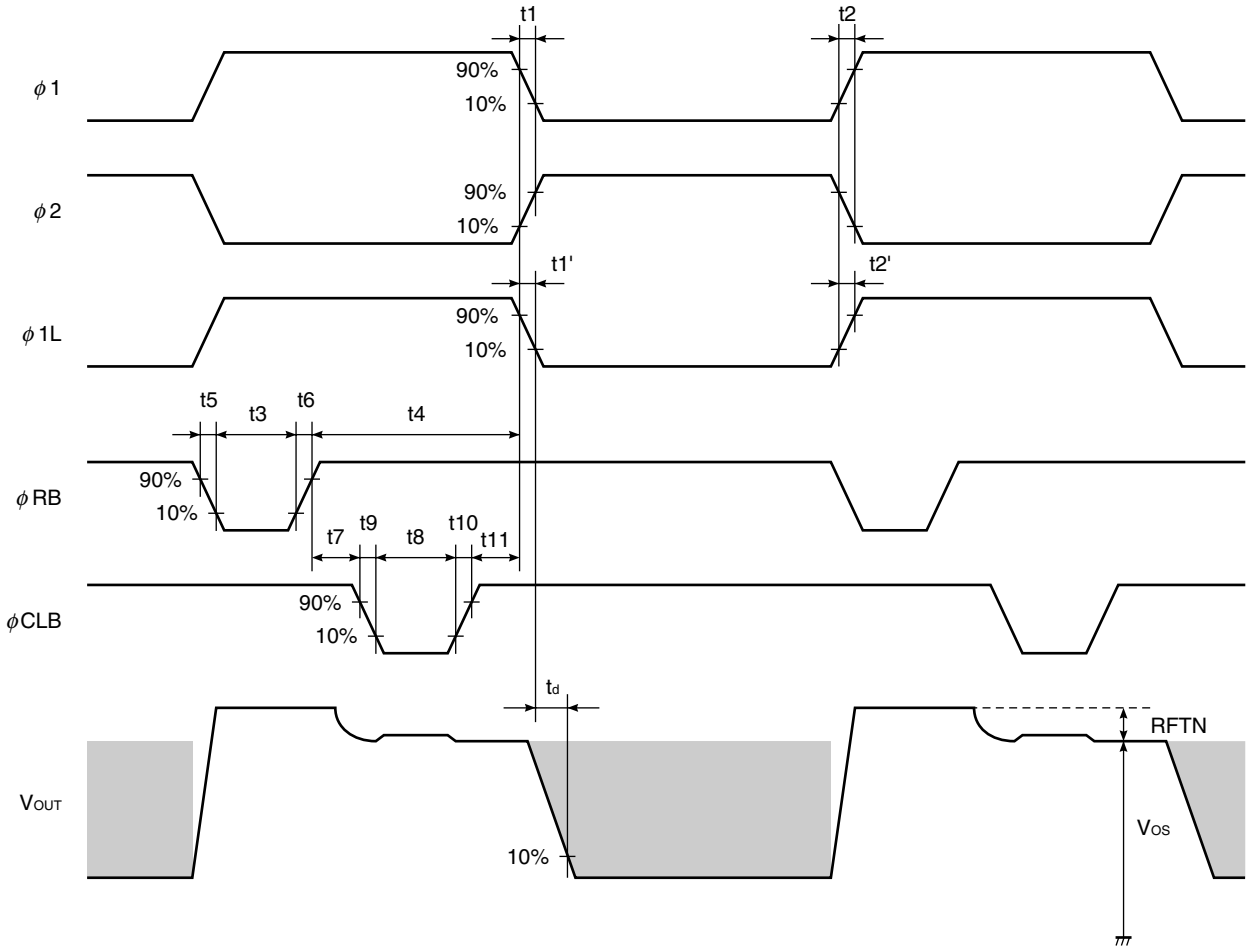
TIMING CHART 1 (for each color)



Note Set the φRB pulse to high level during the φTG1 to φTG3 pulse.
And stop the φRB pulse while the φCLB pulse is low level at line clamp mode.

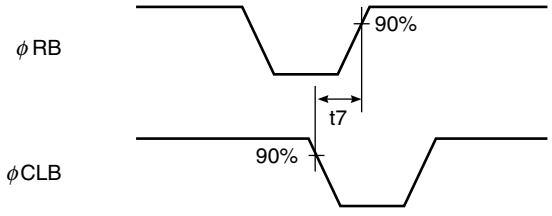
Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB at line clamp mode.

TIMING CHART 2 (Bit clamp mode, for each color)

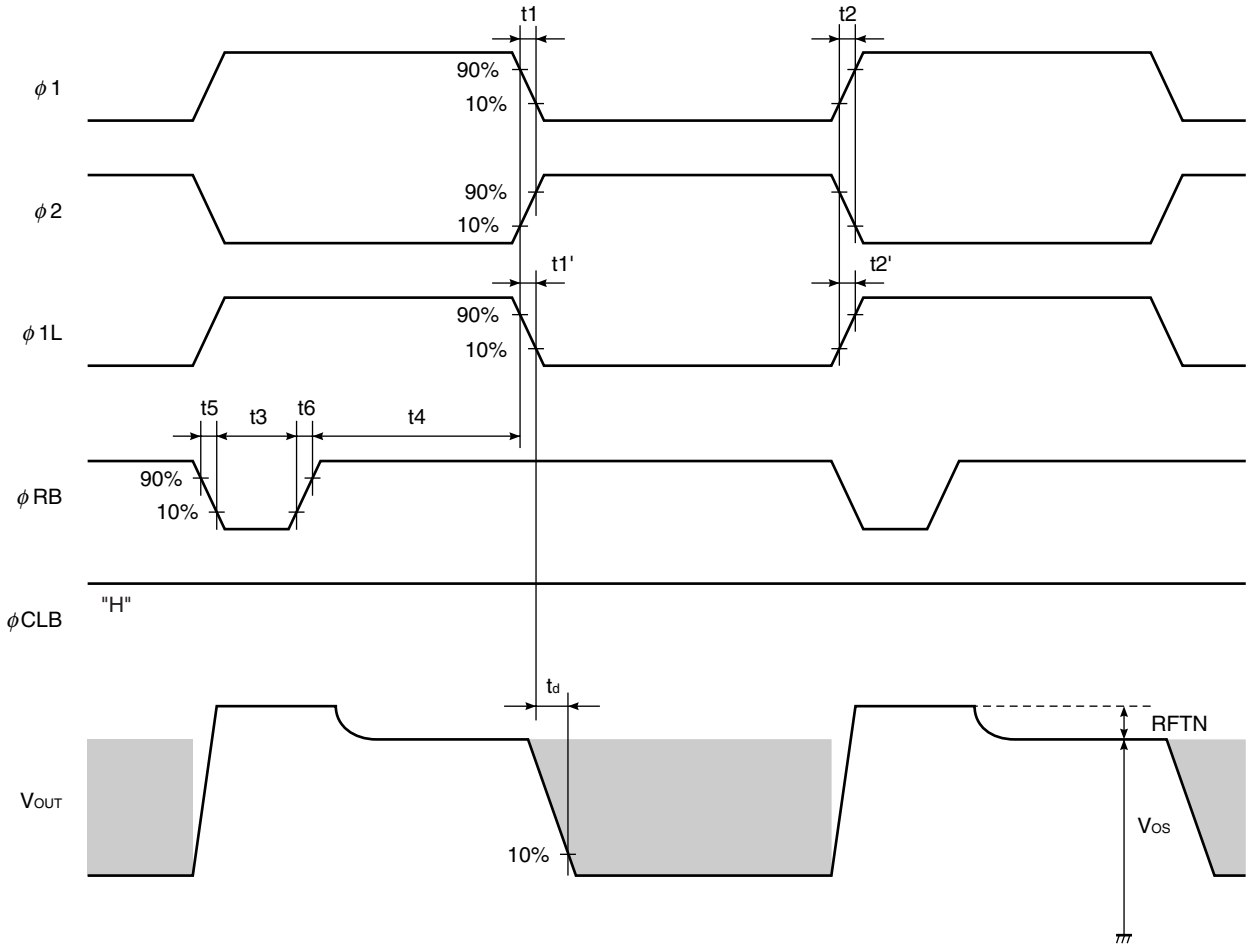


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	100	–	ns
t4	40	150	–	ns
t5, t6	0	25	–	ns
t7	–5 Note	25	–	ns
t8	20	100	–	ns
t9, t10	0	25	–	ns
t11	10	25	–	ns

Note Min. of t7 shows that the φRB and φCLB overlap each other.

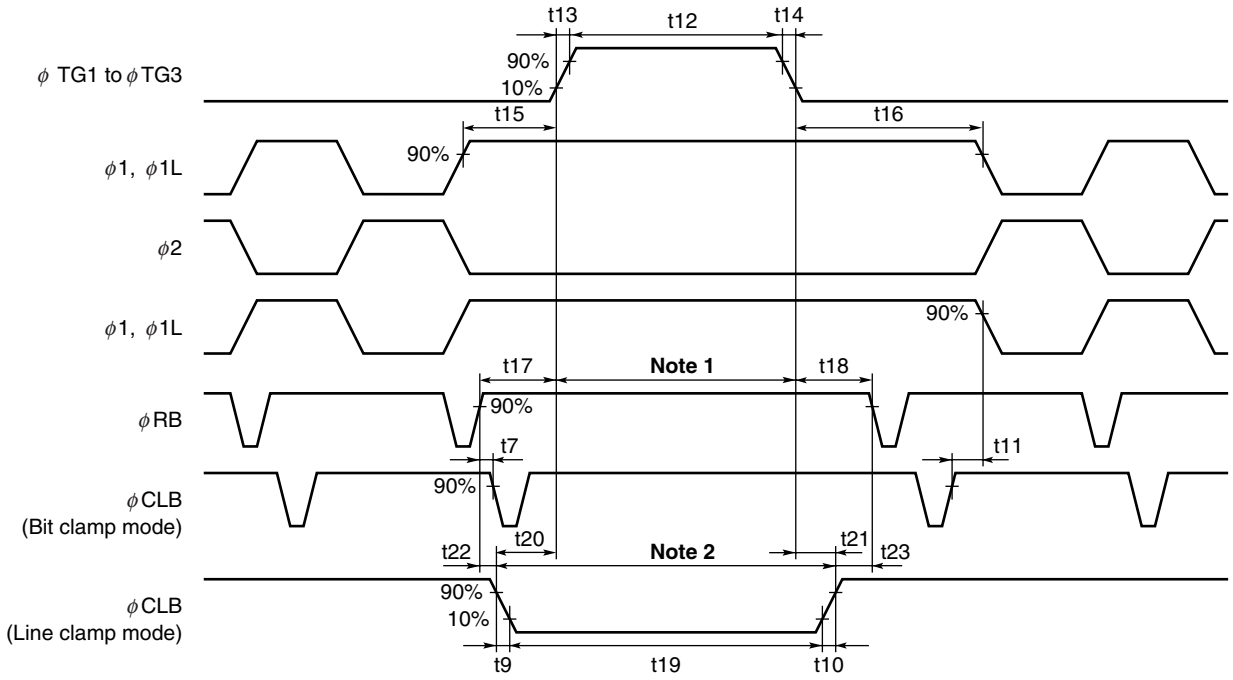


TIMING CHART 3 (Line clamp mode, for each color)



Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	100	–	ns
t4	40	150	–	ns
t5, t6	0	25	–	ns

φTG1 to φTG3, φ1, φ2 TIMING CHART



Symbol	Min.	Typ.	Max.	Unit
t7	–5 Note 3	25	–	ns
t9, t10	0	25	–	ns
t11	10	25	–	ns
t12	5000	10000	50000	ns
t13, t14	0	50	–	ns
t15, t16	900	1000	–	ns
t17, t18	200	400	–	ns
t19	t12	t12	50000	ns
t20, t21	0	50	–	ns
t22, t23	0	350	–	ns

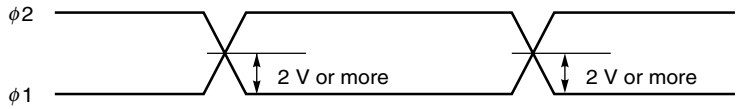
Notes 1. Set the φRB pulse to high level during this period.

2. Stop the φRB pulse during this period.

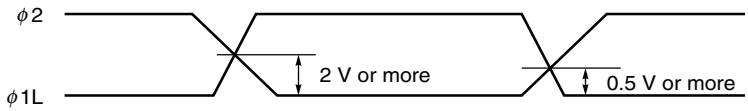
3. Min. of t7 shows that the φRB and φCLB overlap each other.

Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB.

φ1, φ2 cross points



φ1L, φ2 cross points



Remark Adjust cross points (φ1, φ2) and (φ1L, φ2) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**

   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**

   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : **PRNU**

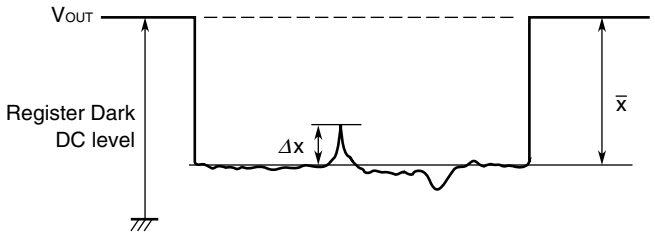
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{10680} x_j}{10680}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**

   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{10680} d_j}{10680}$$

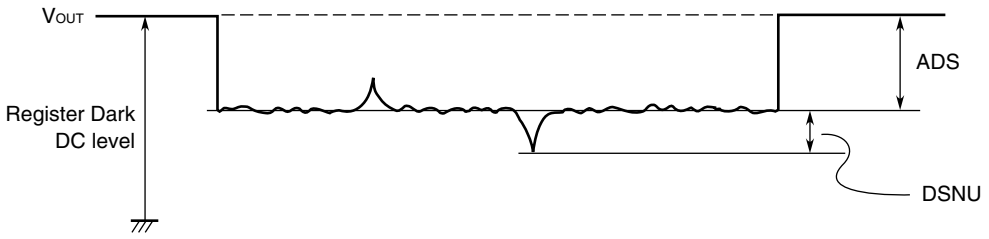
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV) : maximum of $|d_j - ADS|_{j = 1 \text{ to } 10680}$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

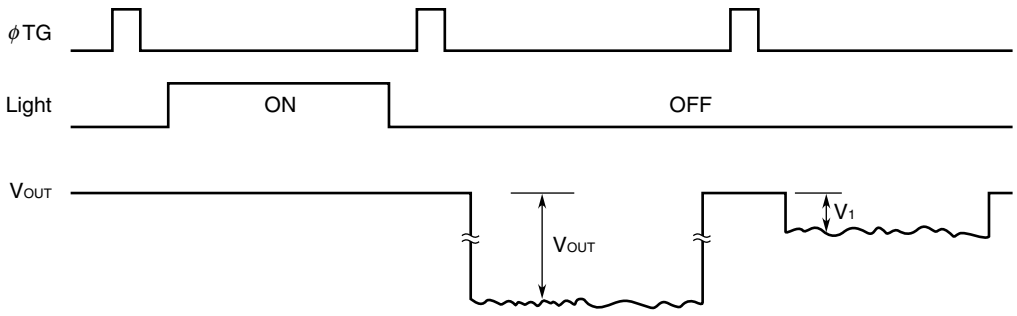
7. Response : **R**

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Random noise (CDS) : **σCDS**

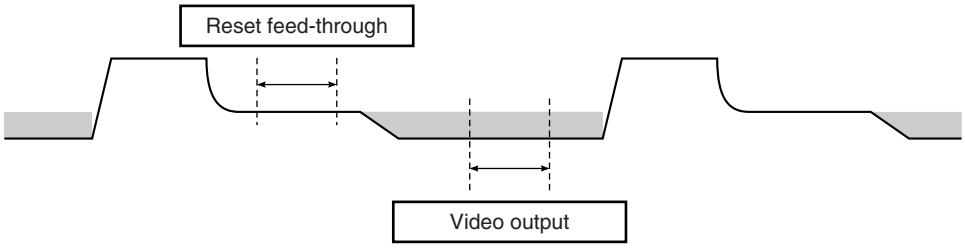
Random noise σCDS is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). σCDS is calculated by the following procedure.

1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get "VD_i".
3. The output level is measured during the video output time averaged over 100 ns to get "VO_i".
4. The correlated double sampling output is defined by the following formula.

$$VCDS_i = VD_i - VO_i$$

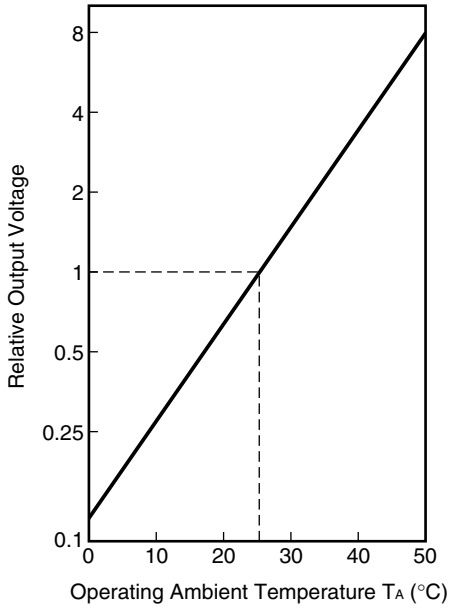
5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σCDS using the following formula equation.

$$\sigma CDS\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (VCDS_i - \overline{V})^2}{100}}\ ,\ \overline{V} = \frac{1}{100}\sum_{i=1}^{100} VCDS_i$$

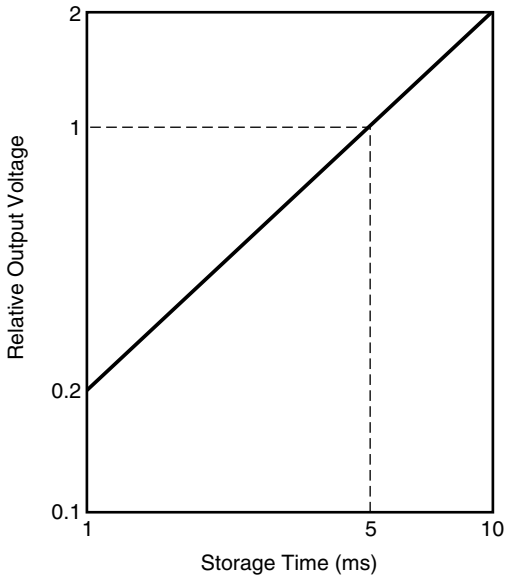


STANDARD CHARACTERISTIC CURVES (Nominal)

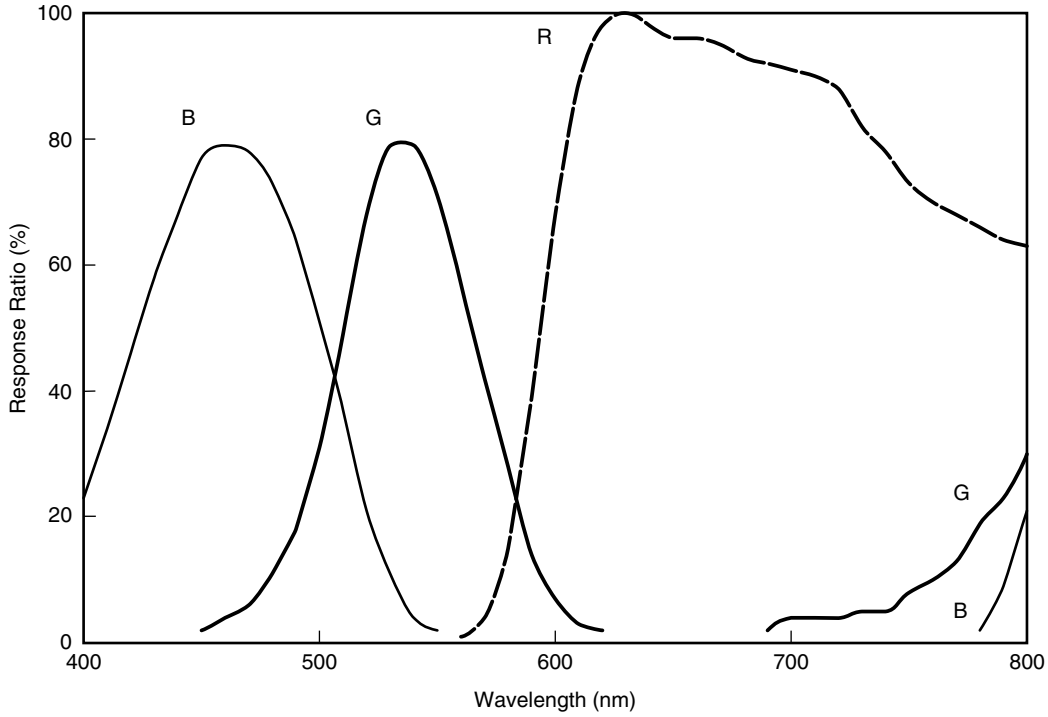
DARK OUTPUT TEMPERATURE CHARACTERISTIC



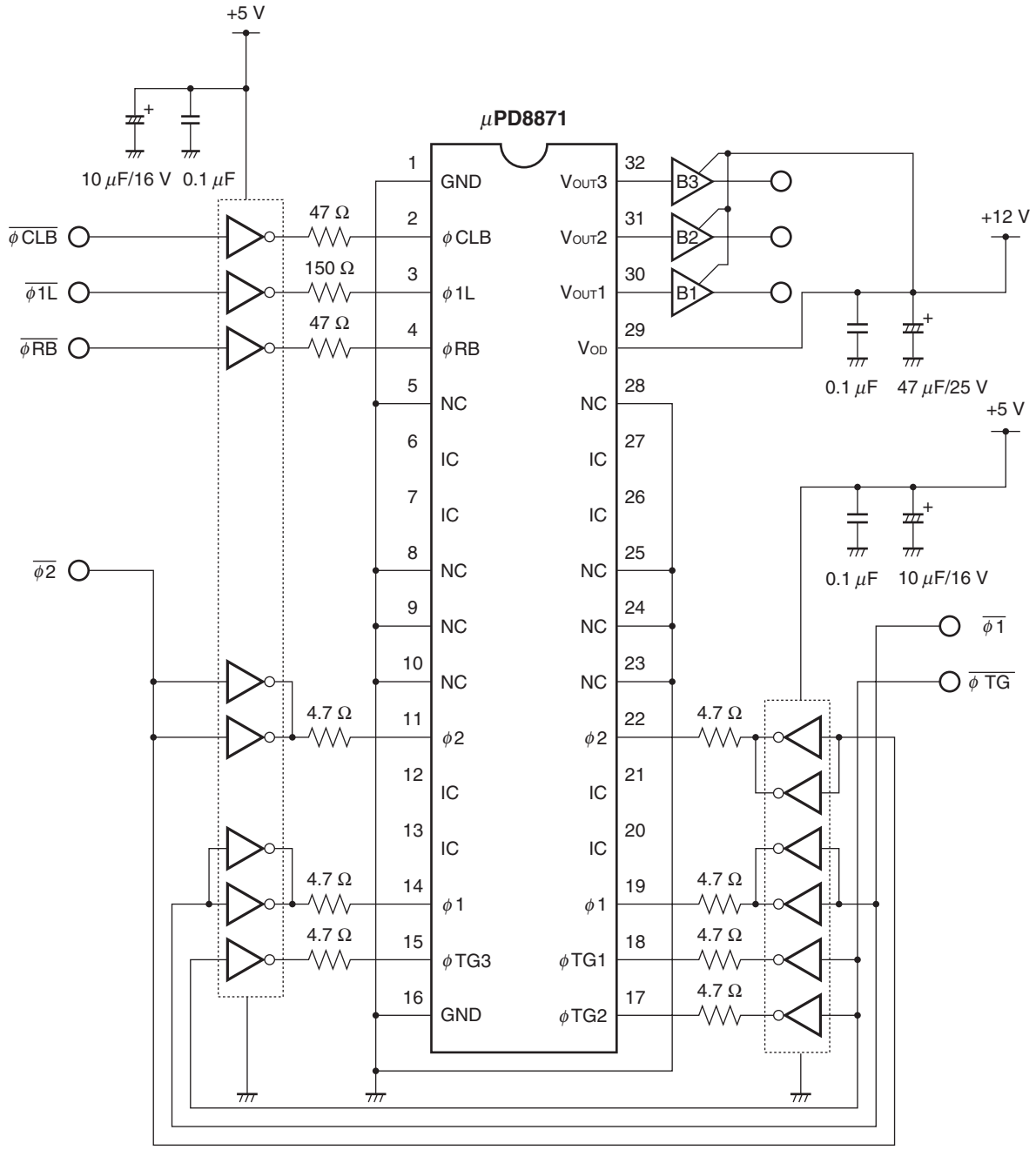
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (T_A = +25°C)

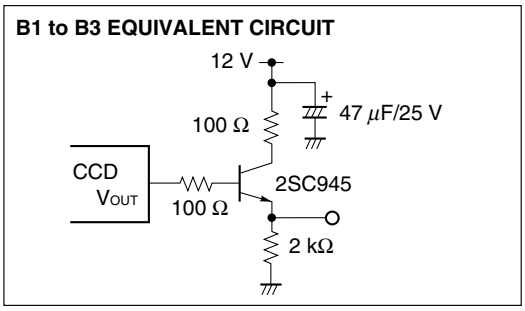


APPLICATION CIRCUIT EXAMPLE



Caution Leave pins 6, 7, 12, 13, 20, 21, 26, 27 (IC) unconnected.

Remark 1. B1 to B3 in the application circuit example are shown in the figure below.



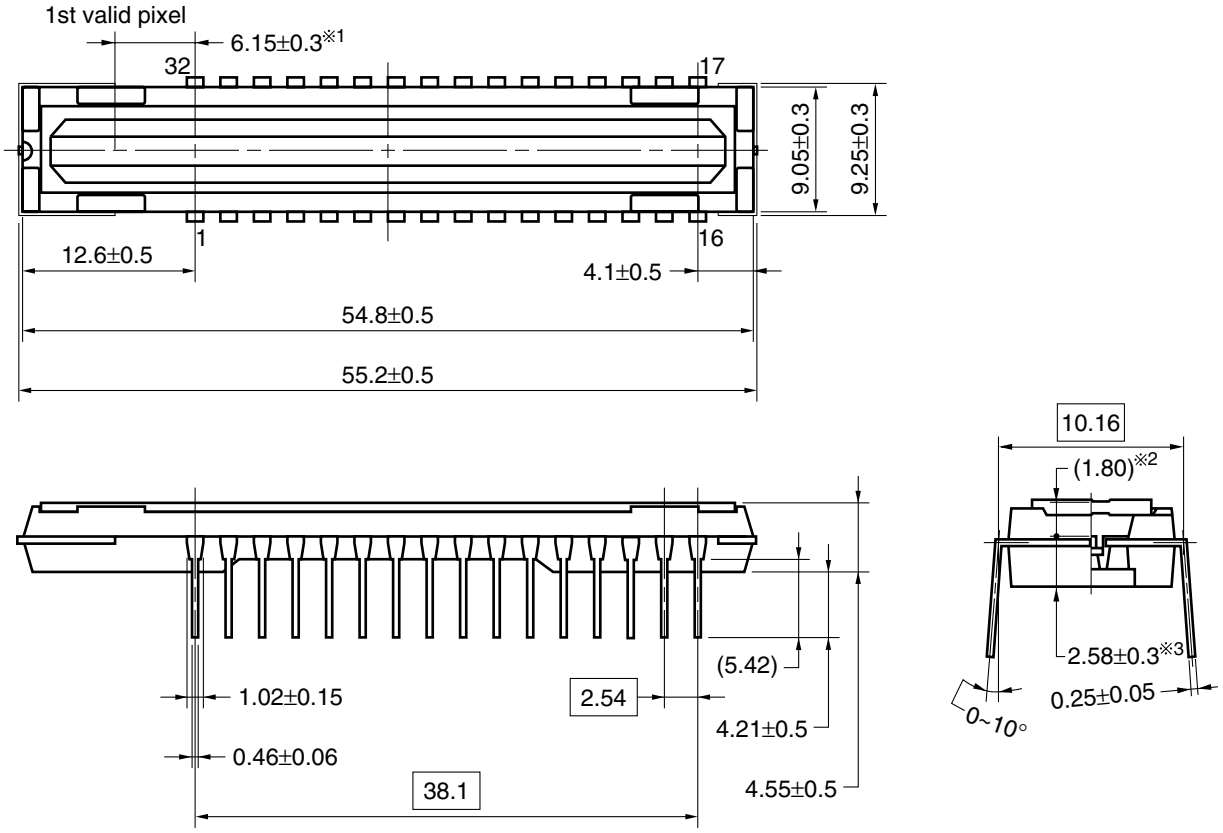
2. Number and type of inverters in the application circuit example are different by data rate.
The following table shows the recommended number and type of inverters for data rate.

Pin Name	Pin No.	Data Rate (MHz)	Inverter	
			Type	Number (each pin)
ϕCLB	2	(data rate) < 10	74HC04	1
ϕ1L	3	(data rate) < 2	74HC04	1
		2 ≤ (data rate) < 10	74AC04	1
ϕRB	4	(data rate) < 10	74HC04	1
ϕ1, ϕ2	14, 19, 11, 22	(data rate) < 2	74HC04	1
		2 ≤ (data rate) < 6	74AC04	1
		6 ≤ (data rate) < 10	74AC04	3
ϕTG1 to ϕTG3	18, 17, 15	(data rate) < 10	74HC04	1

PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 32-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	52.2×6.4×0.7※4	1.5

※1 The 1st valid pixel ⟷ The center of the pin1

※2 The surface of the chip ⟷ The top of the cap

※3 The bottom of the package ⟷ The surface of the chip

※4 Thickness of plastic cap over CCD chip

32C-1CCD-PKG3-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

Type of Through-hole Device

μPD8871CY : CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300°C or below, Heat time : 3 seconds or less (per pin)

Caution During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

NOTES ON CLEANING THE PLASTIC CAP

① CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.
The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

② RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap. Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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