

# OKI Semiconductor

## MSC23V26407TD-xxBS8

2,097,152-Word x 64-Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

### DESCRIPTION

The MSC23V26407TD-xxBS8 is a 2,097,152-word x 64-bit CMOS dynamic random access memory module which is composed of eight 16Mb(2Mx8) DRAMs in TSOP packages mounted with eight decoupling capacitors. This is an 168-pin dual in-line memory module. This module supports any application where high density and large capacity of storage memory are required.

### FEATURES

- 2,097,152-word x 64-bit organization
- 168-pin Dual In-line Memory Module
- Gold tab
- Single 3.3V power supply,  $\pm 0.3V$  tolerance
- Input : LVTTTL compatible
- Output : LVTTTL compatible, 3-state
- Refresh : 2048cycles/ 32ms
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Fast page mode, read modify write capability
- Multi-bit test mode capability
- Serial Presence Detect

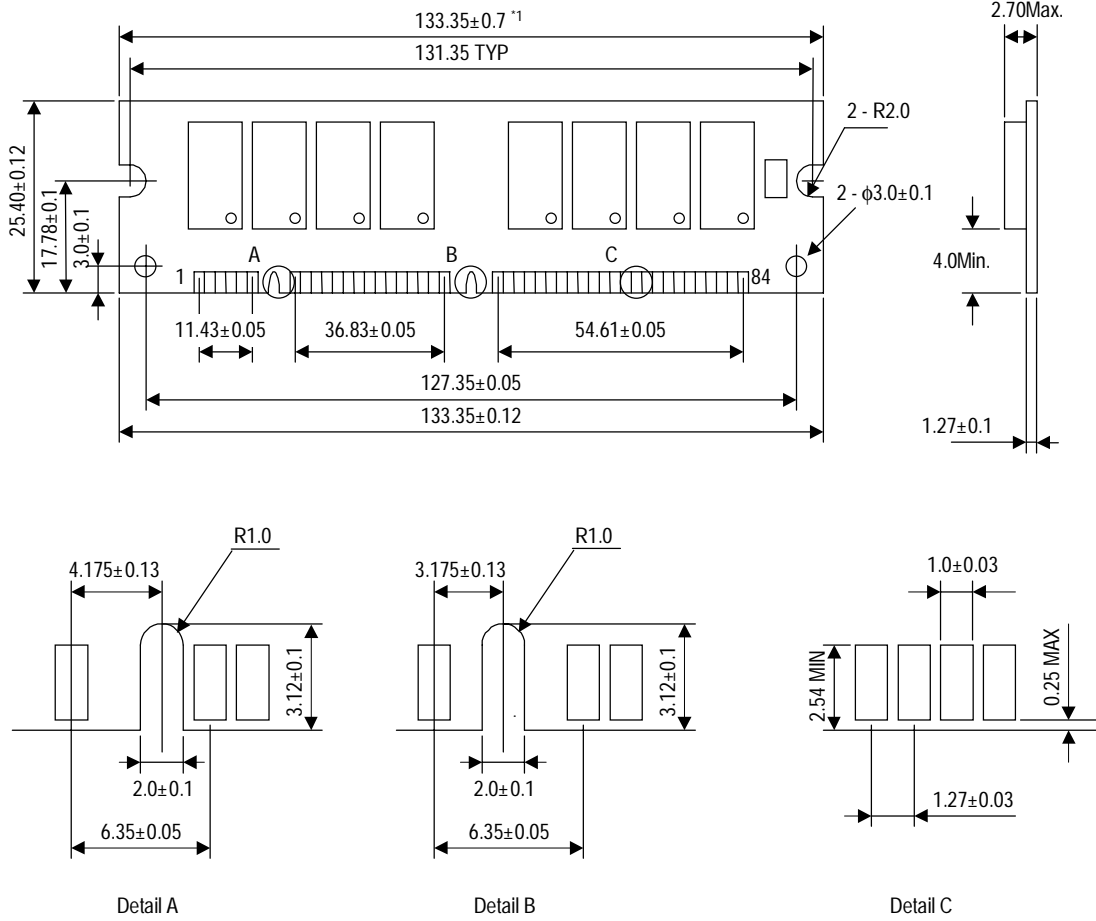
### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation (Max.)	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating	Standby
MSC23V26407TD-50BS8	50ns	25ns	13ns	13ns	90ns	2880mW	14.4mW
MSC23V26407TD-60BS8	60ns	30ns	15ns	15ns	110ns	2592mW	
MSC23V26407TD-70BS8	70ns	35ns	20ns	20ns	130ns	2304mW	

MODULE OUTLINE

MSC23V26407TD-xxBS8

(Unit : mm)



Note:

1. Tolerance over 19.78mm from bottom edge is ±0.7.

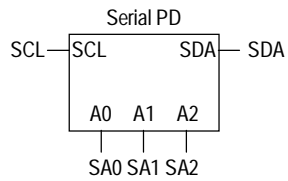
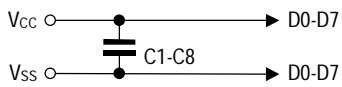
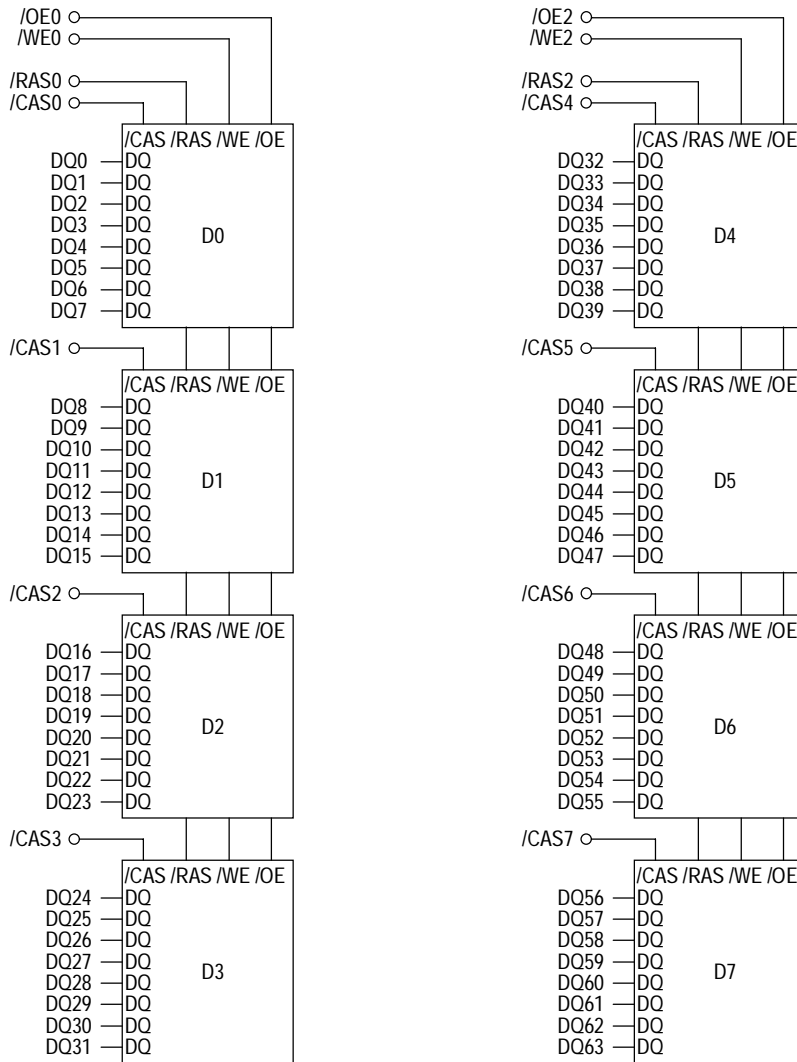
## PIN CONFIGURATION

Front Side		Back Side		Front Side		Back Side	
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>SS</sub>	85	V <sub>SS</sub>	43	V <sub>SS</sub>	127	V <sub>SS</sub>
2	DQ0	86	DQ32	44	/OE2	128	NC
3	DQ1	87	DQ33	45	/RAS2	129	NC
4	DQ2	88	DQ34	46	/CAS2	130	/CAS6
5	DQ3	89	DQ35	47	/CAS3	131	/CAS7
6	V <sub>CC</sub>	90	V <sub>CC</sub>	48	/WE2	132	NC
7	DQ4	91	DQ36	49	V <sub>CC</sub>	133	V <sub>CC</sub>
8	DQ5	92	DQ37	50	NC	134	NC
9	DQ6	93	DQ38	51	NC	135	NC
10	DQ7	94	DQ39	52	NC	136	NC
11	DQ8	95	DQ40	53	NC	137	NC
12	V <sub>SS</sub>	96	V <sub>SS</sub>	54	V <sub>SS</sub>	138	V <sub>SS</sub>
13	DQ9	97	DQ41	55	DQ16	139	DQ48
14	DQ10	98	DQ42	56	DQ17	140	DQ49
15	DQ11	99	DQ43	57	DQ18	141	DQ50
16	DQ12	100	DQ44	58	DQ19	142	DQ51
17	DQ13	101	DQ45	59	V <sub>CC</sub>	143	V <sub>CC</sub>
18	V <sub>CC</sub>	102	V <sub>CC</sub>	60	DQ20	144	DQ52
19	DQ14	103	DQ46	61	NC	145	NC
20	DQ15	104	DQ47	62	NC	146	NC
21	NC	105	NC	63	NC	147	NC
22	NC	106	NC	64	V <sub>SS</sub>	148	V <sub>SS</sub>
23	V <sub>SS</sub>	107	V <sub>SS</sub>	65	DQ21	149	DQ53
24	NC	108	NC	66	DQ22	150	DQ54
25	NC	109	NC	67	DQ23	151	DQ55
26	V <sub>CC</sub>	110	V <sub>CC</sub>	68	V <sub>SS</sub>	152	V <sub>SS</sub>
27	/WE0	111	NC	69	DQ24	153	DQ56
28	/CAS0	112	/CAS4	70	DQ25	154	DQ57
29	/CAS1	113	/CAS5	71	DQ26	155	DQ58
30	/RAS0	114	NC	72	DQ27	156	DQ59
31	/OE0	115	NC	73	V <sub>CC</sub>	157	V <sub>CC</sub>
32	V <sub>SS</sub>	116	V <sub>SS</sub>	74	DQ28	158	DQ60
33	A0	117	A1	75	DQ29	159	DQ61
34	A2	118	A3	76	DQ30	160	DQ62
35	A4	119	A5	77	DQ31	161	DQ63
36	A6	120	A7	78	V <sub>SS</sub>	162	V <sub>SS</sub>
37	A8	121	A9	79	NC	163	NC
38	A10	122	NC	80	NC	164	NC
39	NC	123	NC	81	NC	165	SA0
40	V <sub>CC</sub>	124	V <sub>CC</sub>	82	SDA	166	SA1
41	V <sub>CC</sub>	125	NC	83	SCL	167	SA2
42	NC	126	NC	84	V <sub>CC</sub>	168	V <sub>CC</sub>

## Serial PD Matrix

Byte No.	Function described	SPD Value (Hex)	Note	
0	Number of Byte used	80	128 Bytes	
1	Total SPD Memory size	08	256 Bytes	
2	Memory type	01	Fast Page	
3	Number of Rows	0B	11	
4	Number of Columns	0A	10	
5	Number of Banks	01	1	
6	Module Data Width	40	64	
7	Module Data Width Continued	00	0	
8	Supply Voltage	01	LVTTL	
9	/RAS Access Time	-50	32	50ns
		-60	3C	60ns
		-70	46	70ns
10	/CAS Access Time	-50	0D	13ns
		-60	0F	15ns
		-70	14	20ns
11	DIMM Configuration type	00	Non-Parity	
12	Refresh Rate/Type	00	Normal Refresh	
13	Primary DRAM Width	08	x8	
14	Error Checking DRAM Width	00		
15-61	Superset Information	00	Reserved	
62	SPD Data Revision Code	01	1	
63	Checksum for Byte 0-62	-50	28	
		-60	34	
		-70	43	
64-127	Reserved	00		
128-255	Unused Storage Location (Reserved)	FF		

**BLOCK DIAGRAM**



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to 4.6	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.5 to 4.6	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	8	W
Operating Temperature	$T_{OPR}$	0 to 70	°C
Storage Temperature	$T_{STG}$	-40 to 125	°C

\*  $T_a = 25^\circ\text{C}$

### Recommended Operating Conditions

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V

### Capacitance

( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	$C_{IN1}$	-	49	pF
Input Capacitance (/RAS0, /RAS2, /WE0, /WE2, /OE0, /OE2)	$C_{IN2}$	-	35	pF
Input Capacitance (/CAS0 - /CAS7)	$C_{IN3}$	-	13	pF
I/O Capacitance (DQ0 - DQ63)	$C_{I/O}$	-	13	pF

## DC Characteristics

 $(V_{CC} = 3.3V \pm 0.3V, T_a = 0^\circ C \text{ to } 70^\circ C)$ 

Parameter	Symbol	Condition	-50		-60		-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	$I_{OH} = -2.0mA$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.0mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_{IN} \leq V_{CC}+0.3V$ ; All other pins not under test = 0V	-80	80	-80	80	-80	80	$\mu A$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_{OUT} \leq V_{CC}$	-10	10	-10	10	-10	10	$\mu A$	
Average Power Supply Current (Operating)	$I_{CC1}$	/RAS, /CAS cycling, $t_{RC} = \text{Min.}$	-	800	-	720	-	640	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	/RAS, /CAS = $V_{IH}$	-	16	-	16	-	16	mA	1
		/RAS, /CAS $\geq V_{CC}-0.2V$	-	4	-	4	-	4	mA	
Average Power Supply Current (/RAS only refresh)	$I_{CC3}$	/RAS cycling, /CAS = $V_{IH}$ , $t_{RC} = \text{Min.}$	-	800	-	720	-	640	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	$I_{CC6}$	/RAS cycling, /CAS before /RAS	-	800	-	720	-	640	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	/RAS = $V_{IL}$ , /CAS cycling, $t_{PC} = \text{Min.}$	-	600	-	560	-	520	mA	1, 3

- Notes: 1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.  
2. The address can be changed once or less while /RAS =  $V_{IL}$ .  
3. The address can be changed once or less while /CAS =  $V_{IH}$ .

**AC Characteristics (1/2)**

( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 0^{\circ}C$  to  $70^{\circ}C$ ) Note: 1, 2, 3, 11, 12

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	$t_{RC}$	90	-	110	-	130	-	ns	
Read Modify Write Cycle Time	$t_{RWC}$	131	-	155	-	185	-	ns	
Fast Page Mode Cycle Time	$t_{PC}$	35	-	40	-	45	-	ns	
Fast Page Mode Read Modify Write Cycle Time	$t_{PRWC}$	76	-	85	-	100	-	ns	
Access Time from /RAS	$t_{RAC}$	-	50	-	60	-	70	ns	4, 5, 6
Access Time from /CAS	$t_{CAC}$	-	13	-	15	-	20	ns	4, 5
Access Time from Column Address	$t_{AA}$	-	25	-	30	-	35	ns	4, 6
Access Time from /CAS Precharge	$t_{CPA}$	-	30	-	35	-	40	ns	4
Access Time from /OE	$t_{OEA}$	-	13	-	15	-	20	ns	4
Output Low Impedance Time from /CAS	$t_{CLZ}$	0	-	0	-	0	-	ns	4
/CAS to Data Output Buffer Turn-off Delay Time	$t_{OFF}$	0	13	0	15	0	20	ns	7
/OE to Data Output Buffer Turn-off Delay Time	$t_{OEZ}$	0	13	0	15	0	20	ns	7
Transition Time	$t_T$	3	50	3	50	3	50	ns	3
Refresh Period	$t_{REF}$	-	32	-	32	-	32	ms	
/RAS Precharge Time	$t_{RP}$	30	-	40	-	50	-	ns	
/RAS Pulse Width	$t_{RAS}$	50	10K	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode)	$t_{RASP}$	50	100K	60	100K	70	100K	ns	
/RAS Hold Time	$t_{RSH}$	13	-	15	-	20	-	ns	
/RAS Hold Time referenced to /OE	$t_{ROH}$	13	-	15	-	20	-	ns	
/CAS Precharge Time (Fast Page Mode)	$t_{CP}$	7	-	10	-	10	-	ns	
/CAS Pulse Width	$t_{CAS}$	13	10K	15	10K	20	10K	ns	
/CAS Hold Time	$t_{CSH}$	50	-	60	-	70	-	ns	
/CAS to /RAS Precharge Time	$t_{CRP}$	5	-	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge	$t_{RHCP}$	30	-	35	-	40	-	ns	
/RAS to /CAS Delay Time	$t_{RCD}$	17	37	20	45	20	50	ns	5
/RAS to Column Address Delay Time	$t_{RAD}$	12	25	15	30	15	35	ns	6
Row Address Set-up Time	$t_{ASR}$	0	-	0	-	0	-	ns	
Row Address Hold Time	$t_{RAH}$	7	-	10	-	10	-	ns	
Column Address Set-up Time	$t_{ASC}$	0	-	0	-	0	-	ns	
Column Address Hold Time	$t_{CAH}$	7	-	10	-	15	-	ns	
Column Address to /RAS Lead Time	$t_{RAL}$	25	-	30	-	35	-	ns	
Read Command Set-up Time	$t_{RCS}$	0	-	0	-	0	-	ns	
Read Command Hold Time	$t_{RCH}$	0	-	0	-	0	-	ns	8
Read Command Hold Time referenced to /RAS	$t_{RRH}$	0	-	0	-	0	-	ns	8



**AC Characteristics (2/2)**

( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 0^{\circ}C$  to  $70^{\circ}C$ ) Note: 1, 2, 3, 11, 12

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	$t_{WCS}$	0	-	0	-	0	-	ns	9
Write Command Hold Time	$t_{WCH}$	7	-	10	-	15	-	ns	
Write Command Pulse Width	$t_{WP}$	7	-	10	-	10	-	ns	
/OE Command Hold Time	$t_{OEH}$	13	-	15	-	20	-	ns	
Write Command to /RAS Lead Time	$t_{RWL}$	13	-	15	-	20	-	ns	
Write Command to /CAS Lead Time	$t_{CWL}$	13	-	15	-	20	-	ns	
Data-in Set-up Time	$t_{DS}$	0	-	0	-	0	-	ns	10
Data-in Hold Time	$t_{DH}$	7	-	10	-	15	-	ns	10
/OE to Data-in Delay Time	$t_{OED}$	13	-	15	-	20	-	ns	
/CAS to /WE Delay Time	$t_{CWD}$	36	-	40	-	50	-	ns	9
Column Address to /WE Delay Time	$t_{AWD}$	48	-	55	-	65	-	ns	9
/RAS to /WE Delay Time	$t_{RWD}$	73	-	85	-	100	-	ns	9
/CAS Precharge /WE Delay Time	$t_{CPWD}$	53	-	60	-	70	-	ns	9
/CAS Active Delay Time from /RAS Precharge	$t_{RPC}$	5	-	5	-	5	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	$t_{CSR}$	10	-	10	-	10	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	$t_{CHR}$	10	-	10	-	10	-	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	$t_{WRP}$	10	-	10	-	10	-	ns	
/WE Hold Time from /RAS (/CAS before /RAS)	$t_{WRH}$	10	-	10	-	10	-	ns	
/RAS to /WE Set-up Time (Test Mode)	$t_{WTS}$	10	-	10	-	10	-	ns	
/RAS to /WE Hold Time (Test Mode)	$t_{WTH}$	10	-	10	-	10	-	ns	

- Notes:
1. A start-up delay of 200 $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5$ ns.
  3.  $V_{IH}(\text{Min.})$  and  $V_{IL}(\text{Max.})$  are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF. The output timing reference levels are  $V_{OH} = 2.0$ V and  $V_{OL} = 0.8$ V.
  5. Operation within the  $t_{RCD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  $t_{RCD}(\text{Max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{Max.})$  limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  $t_{RAD}(\text{Max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{Max.})$  limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}(\text{Max.})$  and  $t_{OEZ}(\text{Max.})$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{Min.})$ , then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{Min.})$ ,  $t_{RWD} \geq t_{RWD}(\text{Min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{Min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{Min.})$ , then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  10. These parameters are referenced to the /CAS leading edge in an early write cycle, and to the /WE leading edge in an /OE control write cycle, or a read modify write cycle.
  11. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA9 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low levels. The test mode is cleared and the memory device returned to its normal operating state by performing a /RAS only refresh cycle or a /CAS before /RAS refresh cycle.
  12. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.