
MSM6411A

High speed and Simple 4-Bit Microcontroller

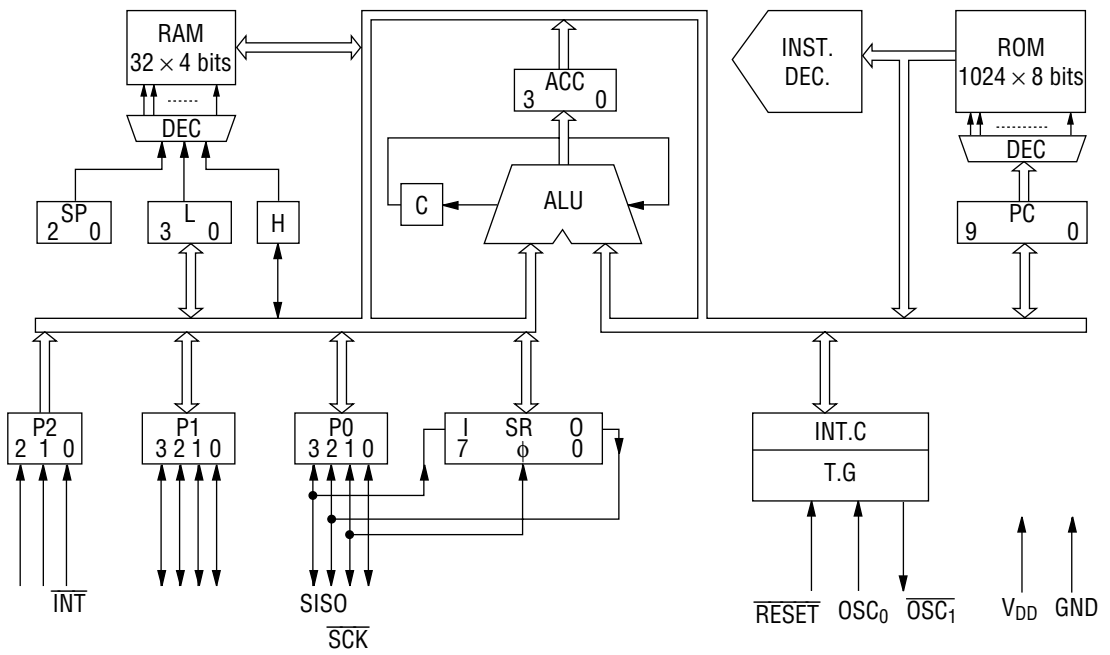
GENERAL DESCRIPTION

The MSM6411A, implemented in complementary metal-oxide semiconductor technology, is a low-power CMOS 4-bit microcontroller developed for smaller-scale control systems.

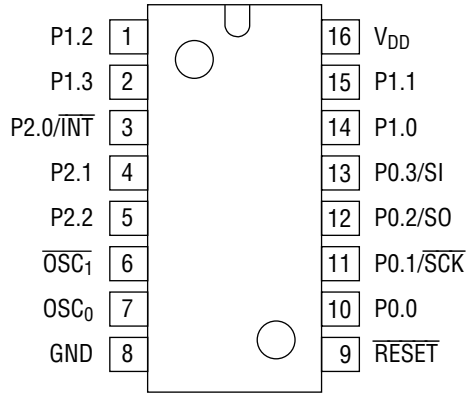
FEATURES

- ROM : 1024 words × 8 bits
- RAM : 32 words × 4 bits
- I/O port
 - Input-output port : 2 ports × 4 bits
 - Input port : 1 port × 3 bits
- 8-bit serial shift register
- 2 interrupt sources (1 external, 1 internal)
- 63 instructions
- Power-down features
- Minimum instruction execution time : 952 ns @ 4.2 MHz clock
- Single 5 V power supply
- Package:
 - 16-pin plastic DIP (DIP16-P-300-2.54) : (Product name : MSM6411A-××RS)
 - ×× indicates a code number.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



16-Pin Plastic DIP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description	During reset
10	P0.0	I/O	4-bit input-output port. P0.1 to P0.3 are used as both input-output ports and shift register pins.	"1"
11	P0.1/SCK			
12	P0.2/SO			
13	P0.3/SI			
14	P1.0	I/O	4-bit input-output port.	"1"
15	P1.1			
1	P1.2			
2	P1.3			
3	P2.0/INT	I	3-bit input port with latch. P2.0 is used as both input port and INT input pin (falling edge trigger input).	Latch is reset. ("0")
4	P2.1			
5	P2.2			
7	OSC ₀	I	System clock input pin.	Clocked in
6	OSC ₁	O	System clock output pin. This pin and OSC ₀ pin make up the oscillator circuit.	—
9	RESET	I	Input pin for system reset.	—
16	V _{DD}	I	Power supply voltage pin.	—
8	GND	I	Ground pin.	—

INSTRUCTION LIST

	Mnemonic	Code	Byte	Cycle	Description
Load, Push, Pop, Exchange	LAI n	90-9F	1	1	$A \leftarrow n$
	LLI n	80-8F	1	1	$L \leftarrow n$
	LHLI nn	15nn	2	2	$HL \leftarrow nn$
	LAL	21	1	1	$A \leftarrow L$
	LLA	2D	1	1	$L \leftarrow A$
	LAM	38	1	1	$A \leftarrow M$
	LMA	2F	1	1	$M \leftarrow A$
	LAMD mm	10mm	2	2	$A \leftarrow Md$
	LMAD mm	11mm	2	2	$Md \leftarrow A$
	LMSR	3E5A	2	2	$M(w) \leftarrow SR$
	LSRM	3E52	2	2	$SR \leftarrow M(w)$
	PUSH	1C	1	3	$ST \leftarrow C, A, H, L, SP \leftarrow SP - 1$
	POP	1D	1	3	$C, A, H, L \leftarrow ST, SP \leftarrow SP + 1$
	X	28	1	1	$A \leftarrow M$
Increment and Decrement	INL	31	1	1	$L \leftarrow L + 1, \text{SKIP IF } L = "0"$
	INH	32	1	1	$H \leftarrow H + 1, \text{SKIP IF } H = "0"$
	INM	33	1	1	$M \leftarrow M + 1, \text{SKIP IF } M = "0"$
	INMD mm	12mm	2	2	$Md \leftarrow Md - 1, \text{SKIP IF } Md = "0"$
	DCL	35	1	1	$L \leftarrow L - 1, \text{SKIP IF } L = "F"$
	DCH	36	1	1	$H \leftarrow H - 1$
	DCM	37	1	1	$M \leftarrow M - 1, \text{SKIP IF } M = "F"$
Arithmetic	ADS	02	1	1	$A \leftarrow A + M, \text{SKIP IF } Cy = "1"$
	ADC	03	1	1	$C, A \leftarrow C + A + M$
	AIS n	3E4n	2	2	$A \leftarrow A + n, \text{SKIP IF } Cy = "1"$
	DAS	0A	1	1	$A \leftarrow A + 10$
	AND	0D	1	1	$A \leftarrow A \wedge M$
	EOR	04	1	1	$A \leftarrow A \vee M$
	CMA	0B	1	1	$A \leftarrow \bar{A}$
	CAM	16	1	1	SKIP IF $A = M$
	SC	07	1	1	$C \leftarrow "1"$
	RC	08	1	1	$C \leftarrow "0"$
	TC	09	1	1	SKIP IF $C = "1"$
RAL	0E	1	1	$C \leftarrow 3 \leftarrow 2 \leftarrow 1 \leftarrow 0 \leftarrow \overbrace{A}$	

INSTRUCTION LIST (continued)

	Mnemonic	Code	Byte	Cycle	Description
Bit manipulation	TAB n2	54-57	1	1	SKIP IF [A bit n2] = "1"
	TMB n2	58-5B	1	1	SKIP IF [M bit n2] = "1"
	RMB n2	68-6B	1	1	[M bit n2]←"0"
	SMB n2	78-7B	1	1	[M bit n2]←"1"
	TPBD p•n2	3D p0 to 3	2	2	SKIP IF [Pp bit n2] = "1"
	RPBD p•n2	3D p4 to 7	2	2	[Pp bit n2]←"0"
	SPBD p•n2	3D p8 to B	2	2	[Pp bit n2]←"1"
Interrupt	MEI	3E60	2	2	MEIF←"1"
	MDI	3E61	2	2	MEIF←"0"
	EICT	3DCB	2	2	EICTF←"1"
	EIEX	3DC8	2	2	EIEXF←"1"
	DICT	3DC7	2	2	EICTF←"0"
	DIEX	3DC4	2	2	EIEXF←"0"
	TICT	3DC3	2	2	SKIP IF EICTF = "1"
	TIEX	3DC0	2	2	SKIP IF EIEXF = "1"
	TQEX	3D20	2	2	SKIP IF IRQEX = "1"
	TQSR	3DD3	2	2	SKIP IF IRQSR = "1"
	RQEX	3D24	2	2	IRQEX←"0"
	RQSR	3DD7	2	2	IRQSR←"0"
Shift register	ESR	3DBA	2	2	SRF←"1"
	DSR	3DB6	2	2	SRF←"0"
	TSR	3DB2	2	2	SKIP IF SRF = "1"
Branch	JCP a ₆	C0 to FF	1	1	PC←a ₆
	JP a ₁₀	40 to 43 00 to FF	2	2	PC←a ₁₀
	CAL a ₁₀	A0 to A3 00 to FF	2	4	ST←PC + 2, PC←a ₁₀ , SP←SP - 1
Input/output	RT	IE	1	4	PC←ST, SP←SP + 1
	IPD p	3DpD	2	2	A←Pp
	OPD p	3DpC	2	2	Pp←A
CPU control	STOP	3DB9	2	2	STOP CLOCK
	NOP	00	1	1	NO OPERATION

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +7	V
Input Voltage	V_I		-0.3 to V_{DD}	V
Output Voltage	V_O		-0.3 to V_{DD}	V
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$ per package	200 max.	mW
		$T_a = 25^\circ\text{C}$ per output	50 max.	mW
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	$f_{osc} \leq 1 \text{ MHz}$	3 to 6	V
		$f_{osc} \leq 4.2 \text{ MHz}$	4.5 to 5.5	V
Data-Hold Voltage	V_{DDH}	$f_{osc} \leq 0 \text{ Hz}$	2 to 6	V
Operating Temperature	T_{op}	—	-40 to +85	$^\circ\text{C}$
Fan Out	N	MOS load	15	—
		TTL load	1	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5 V ±10%, T_a = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1,*2	V _{IH}	—	2.4	—	V _{DD}	V
"H" Input Voltage *3,*4	V _{IH}	—	3.6	—	V _{DD}	V
"L" Input Voltage	V _{IL}	—	-0.3	—	+0.8	V
"H" Output Voltage *1,*5	V _{OH}	I _O = -15 μA	4.2	—	—	V
"L" Output Voltage *1	V _{OL}	I _O = 1.6 mA	—	—	0.4	V
"L" Output Voltage *5	V _{OL}	I _O = 15 μA	—	—	0.4	V
Input Current *3	I _{IH} /I _{IL}	V _I = V _{DD} /0 V	—	—	15/-15	μA
Input Current *2,*4	I _{IH} /I _{IL}	V _I = V _{DD} /0 V	—	—	1/-30	μA
"H" Output Current *1	I _{OH}	V _O = 2.4 V	-0.1	—	—	mA
"H" Output Current *1	I _{OH}	V _O = 0.4 V	—	—	-1.2	mA
Input Capacitance	C _I	f = 1 MHz, T _a = 25°C	—	5	—	pF
Output Capacitance	C _O		—	7	—	
Power Supply Current (In Stop Mode)	I _{DDs}	V _{DD} = 2 V, no load, T _a = 25°C	—	0.2	5	μA
		No load	—	1	100	μA
Power Supply Current	I _{DD}	Crystal oscillation, no load, 4.2 MHz	—	6	12	mA

*1 Applied to P0 and P1

*2 Applied to P2

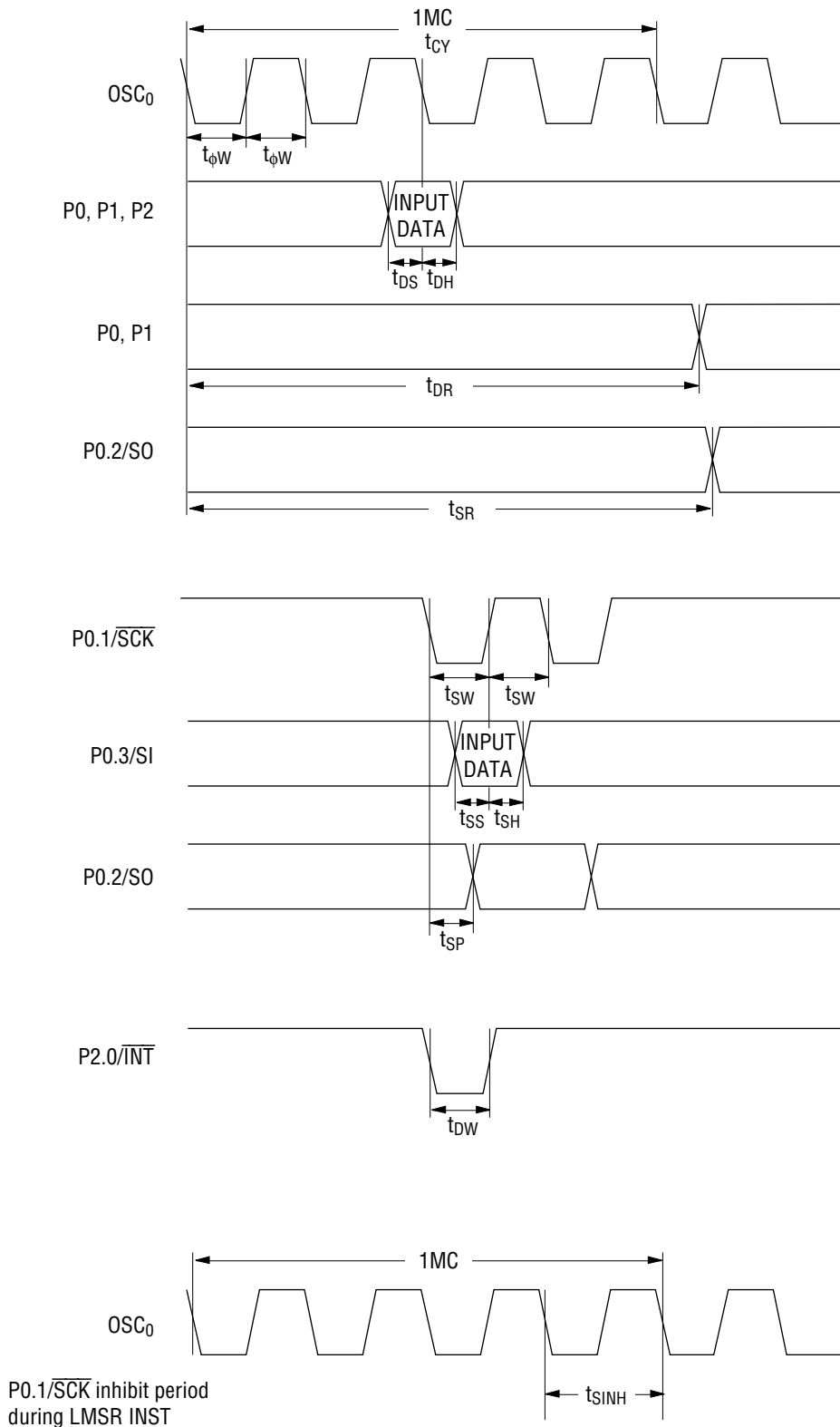
*3 Applied to OSC₀*4 Applied to $\overline{\text{RESET}}$ *5 Applied to $\overline{\text{OSC}}_1$

AC Characteristics

 $(V_{DD} = 5\text{ V} \pm 10\%, T_a = -40\text{ to }+85^\circ\text{C})$

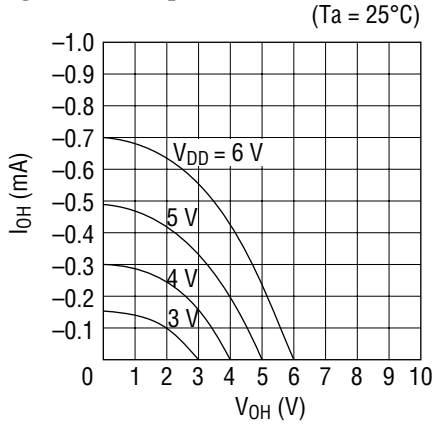
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (OSC ₀) Pulse Width	$t_{\phi W}$	—	119	—	—	ns
Cycle Time	t_{CY}	—	952	—	—	ns
Input Data Setup Time	t_{DS}	—	120	—	—	ns
Input Data Hold Time	t_{DH}	—	120	—	—	ns
Input Data/Input Clock Pulse Width	t_{DW}	—	120	—	—	ns
SR Clock Pulse Width	t_{SW}	—	$t_{\phi W}$	—	—	ns
SR Data Setup Time	t_{SS}	—	120	—	—	ns
SR Data Hold Time	t_{SH}	—	120	—	—	ns
Data Delay Time	t_{DR}	$C_L = 15\text{ pF}$	—	—	$t_{CY} + 300$	ns
PORT Clock SR Data Delay Time	t_{SR}	$C_L = 15\text{ pF}$	—	—	$t_{CY} + 480$	ns
External Clock SR Data Delay Time	t_{SP}	$C_L = 15\text{ pF}$	—	—	360	ns
SR Clock Invalid Time	t_{SINH}	—	$2/8 t_{CY}$	—	—	ns

Timing Diagrams

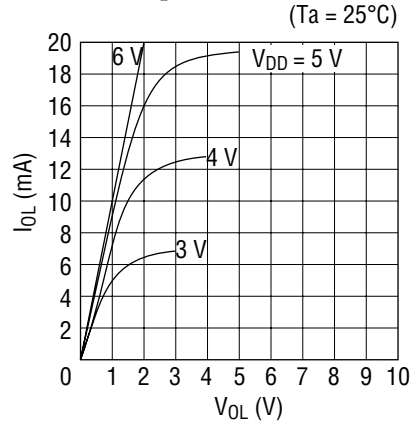


Operating Characteristics

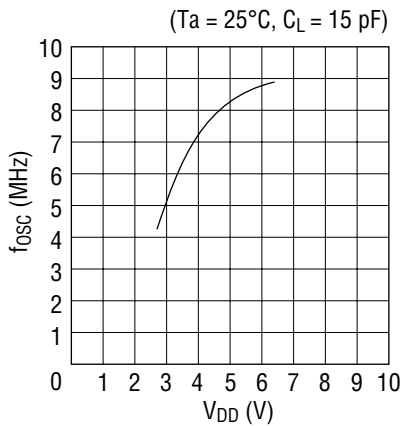
Current (I_{OH}) vs. Voltage (V_{OH}) for High State Output



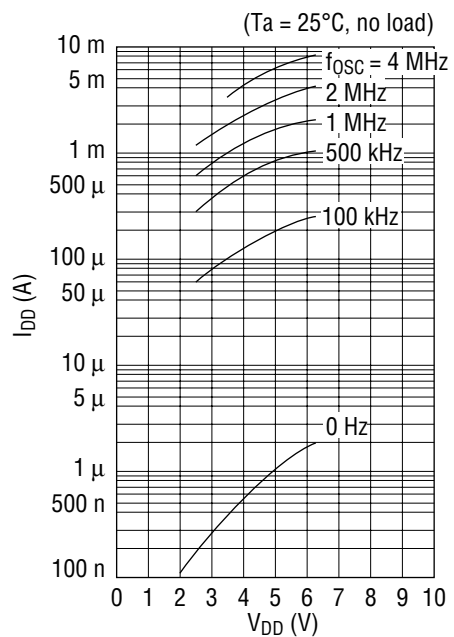
Current (I_{OL}) vs. Voltage (V_{OL}) for Low State Output



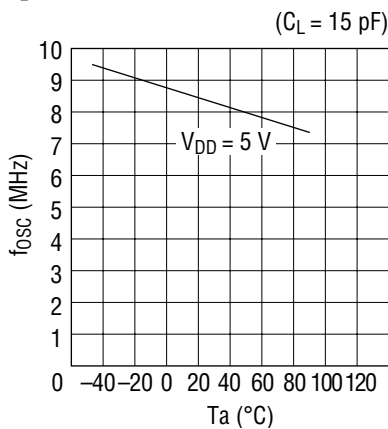
Maximum Clock Frequency (f_{OSC}) vs. Supply Voltage (V_{DD})



Supply Current (I_{DD}) vs. Supply Voltage (V_{DD})



Maximum Clock Frequency (f_{OSC}) vs. Temperature (T_a)



PACKAGE DIMENSIONS

(Unit : mm)

