E2E0040-27-Y3

OKI Semiconductor

This version: Jan. 1998
Previous version: Mar. 1996

MSM64431

Built-in 8-Bit A/D Converter 4-Bit Microcontroller

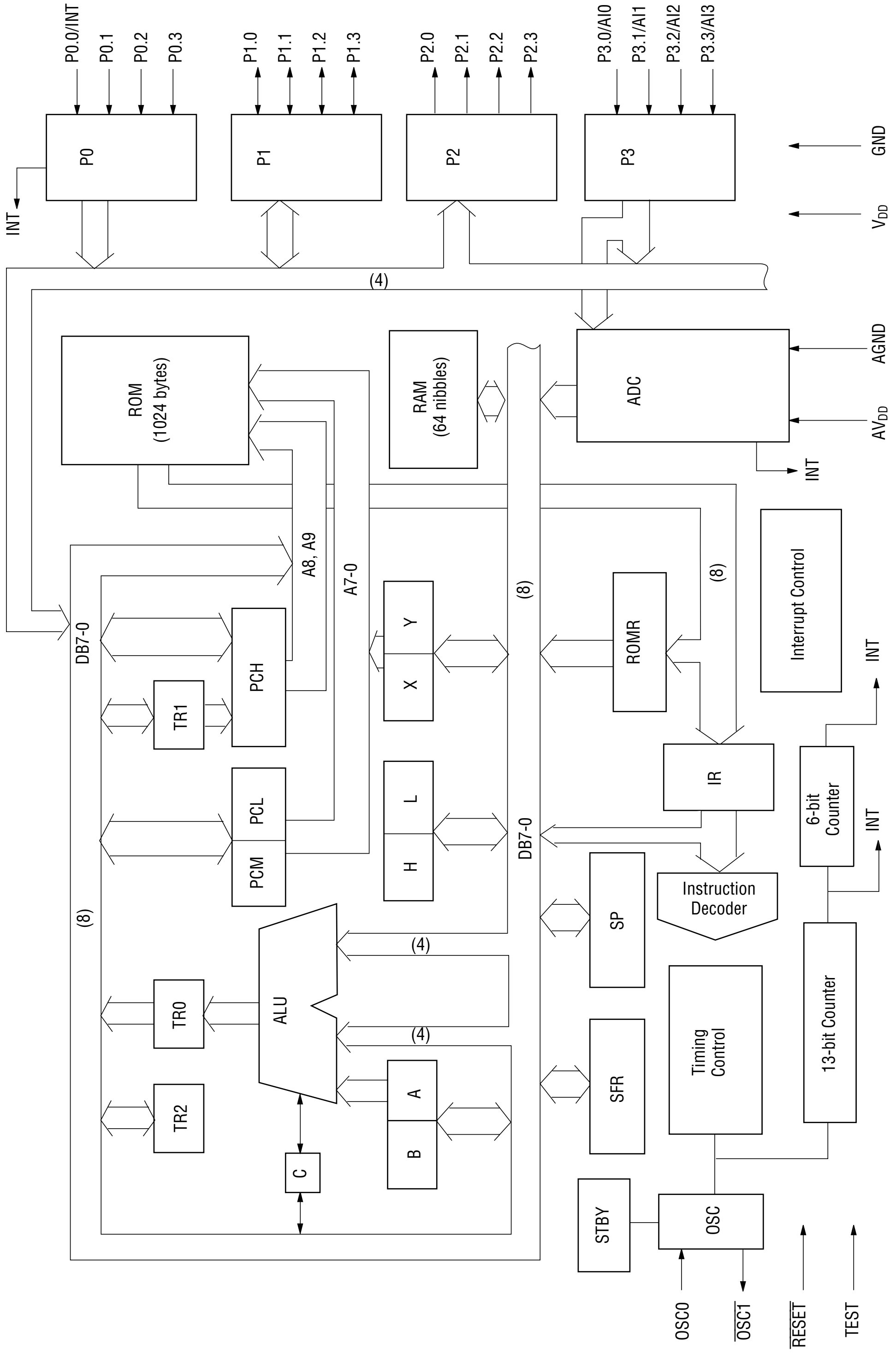
GENERAL DESCRIPTION

The MSM64431 is a high-performance 4-bit microcontroller that incorporates OKI's nX-4/20 CPU core.
The MSM64431 has a minimum instruction execution time of 714 ns (@4.2 MHz) and contains a 1024-byte program memory, a 64-nibble data memory, four I/O ports (16 bits in total) , an 8-bit 4-channel A/D converter, and a time base counter.
Applications include various types of controllers, remote-controllers, home appliances such as fans, and toys.

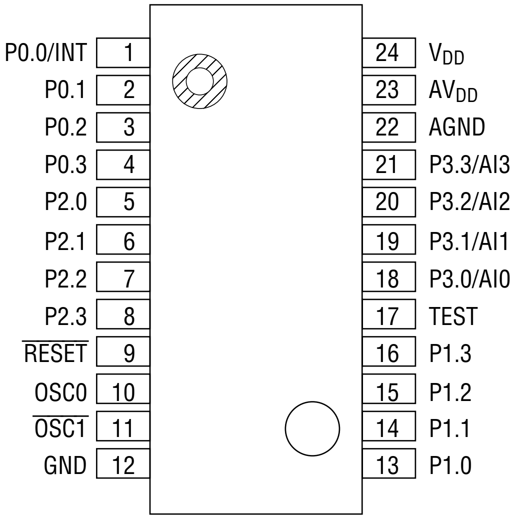
FEATURES

• Operating range	
Operating frequency	: 500 kHz to 4.2 MHz
Operating voltage	: 4.5 to 5.5 V
Operating temperature	: -40 to +85°C
• Internal program memory	: 1024 bytes
• Internal data memory	: 64 nibbles
• Minimum instruction execution time	: 714 ns @ 4.2 MHz
• A/D converter	: 8-bit; 4 channels
• I/O port	
Input-output port	: 1 port × 4 bits
Input port	: 2 ports × 4 bits
Output port	: 1 port × 4 bits
• External interrupt	: 1
• Interrupt sources	: 4
• Package options:	
24-pin plastic DIP (DIP24-P-600-2.54)	: (Product name : MSM64431-×××RS)
24-pin plastic SOP (SOP24-P-430-1.27-K)	: (Product name : MSM64431-×××GS-K)
	××× indicates the code number.

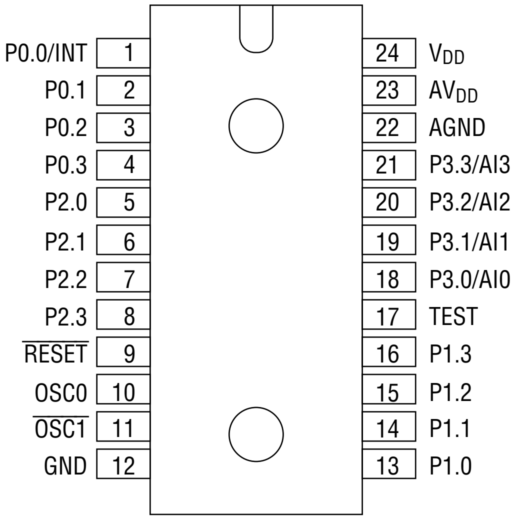
BLOCK DIAGRAM



PIIN CONFIGURATION (TOP VIEW)



24-Pin Plastic SOP



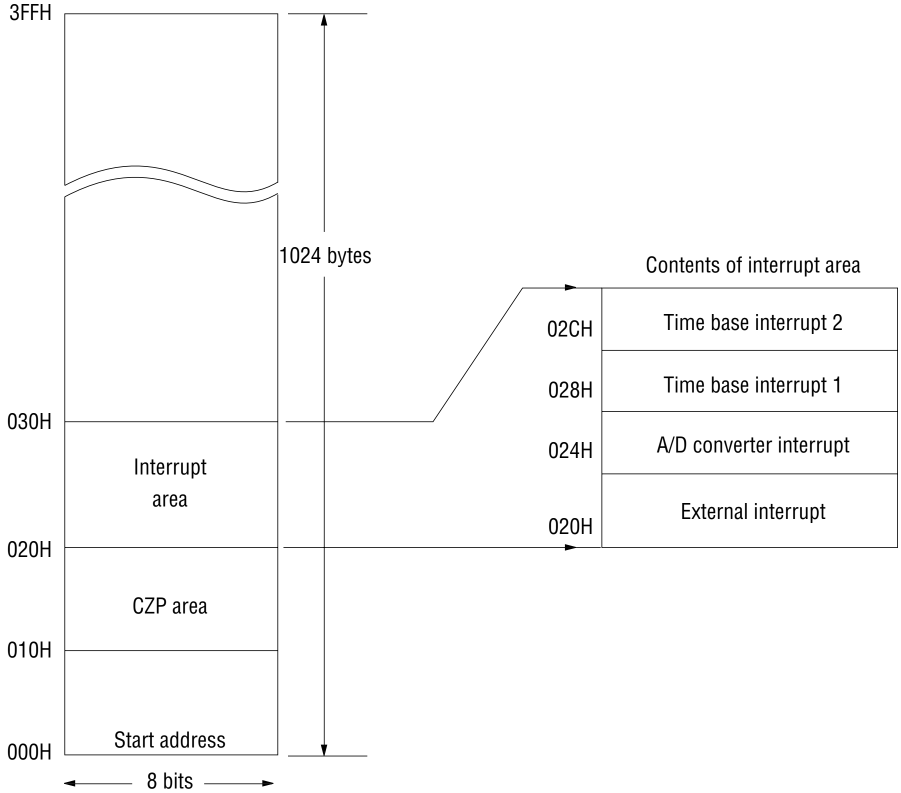
24-Pin Plastic DIP

PIN DESCRIPTIONS

Function	Symbol	Type	Description
Power supply	V_{DD}	—	+5 V digital power supply
	GND	—	0 V digital ground
	AV_{DD}	—	+5 V analog power supply
	AGND	—	0 V analog ground
Oscillation	OSC0	I	Oscillation input/external clock input
	$\overline{\text{OSC1}}$	O	Oscillation output
Control	$\overline{\text{RESET}}$	I	System reset (starts from address 0)
	TEST	I	Test only input
Ports	PORT 0	I	4-bit input port. P0.0's secondary function is an external interrupt input.
	PORT 1	I/O	4-bit input-output port
	PORT 2	O	4-bit output port
	PORT 3	I	4-bit input port. This port becomes an analog input channel at A/D conversion when set to perform its secondary function.

MEMORY MAPS

Program Memory

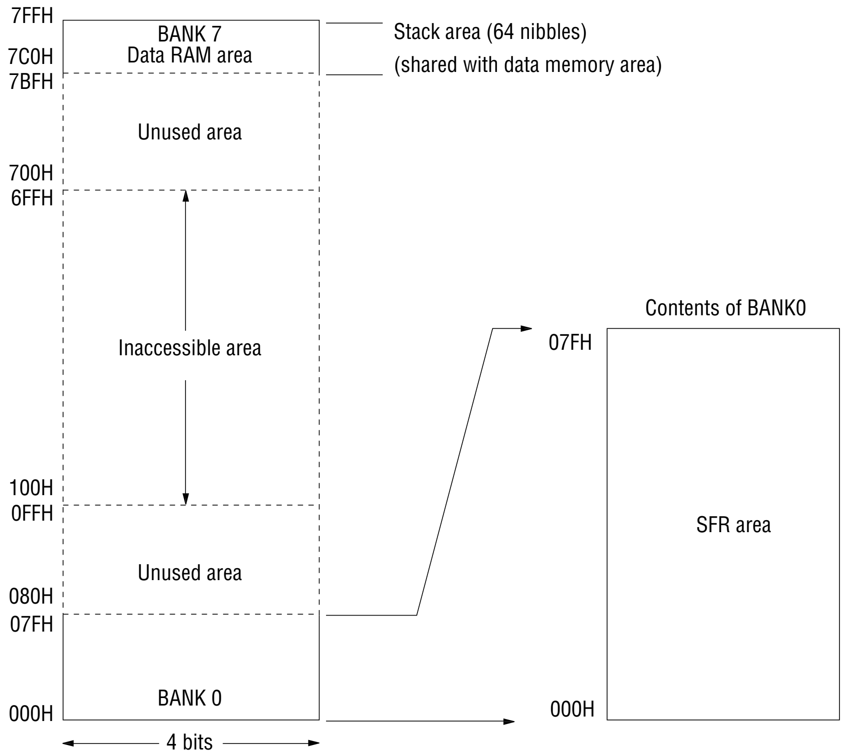


Program Memory Map

Address 000H is the instruction execution start address after system reset.
The CZP area from address 010H to address 01FH is the start address area for the CZP subroutine of one-byte call instruction.
The interrupt address from address 020H to 03DH is assigned the start address of interrupt subroutines.

Data Memory

Data memory is composed of eight banks with 256 nibbles (256 x 4 bits) in each bank. In data RAM, BANK 7 is assigned 64 nibbles and BANK 0 is assigned to Special Function Registers.



Data memory map

The stack area is memory that starts at address 7FFH and extends downwards.
Four nibbles are used by subroutine call instructions and eight nibbles are used when interrupts are generated.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	$V_{DD} = AV_{DD}$	Ta = 25°C GND = AGND = 0 V	–0.3 to 7.0	V
Input voltage	V_I		–0.3 to V_{DD}+0.3	
Output voltage	V_O		–0.3 to V_{DD}+0.3	
Analog input voltage	V_{AI}		–0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	$V_{DD} = AV_{DD}$	f = 500 kHz to 4.2 MHz	4.5 to 5.5	V
Operating temperature	T_{op}	—	–40 to +85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = AV_{DD} = 5 V ± 10%, GND = AGND = 0 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH1}	—	0.5 V_{DD}	—	V_{DD}	V
"H" input voltage *2	V_{IH2}	—	0.7 V_{DD}	—	V_{DD}	V
"L" input voltage *3	V_{IL}	—	0	—	0.2 V_{DD}	V
"H" output current *4	I_{OH}	V_{OH} = V_{DD}–1.0 V	1.0	—	—	mA
"L" output current *4	I_{OL1}	V_{OL1} = 0.4 V	–1.6	—	—	mA
"L" output current *5	I_{OL2}	V_{OL2} = 1.2 V	–10	—	—	mA
input leakage current *6	I_{LI}	V_I = V_{DD}/0 V	—	—	±5	µA
Output leakage current *5	I_{LO}	V_I = V_{DD}/0 V	—	—	±5	µA
Pull-up resistance *7	R_{PU}	—	20	40	80	kΩ
Pull-down resistance *8	R_{PD}	—	2	5	15	kΩ
Analog reference power supply current *3	I_{REF}	V_{DD} = AV_{DD} = 5 V GND = AGND = 0 V	—	0.5	2.0	mA
Operating current consumption	I_{DD}	V_{DD} = AV_{DD} = 5 V f=4.2 MHz (no load)	—	—	3	mA
Current consumption at HALT *9	I_{DDH}	V_{DD} = AV_{DD} = 5 V f=4.2 MHz (no load)	—	—	300	µA
Stand-by current *9	I_{DDS}	V_{DD} = AV_{DD} = 2 V Ta = 25°C	—	—	2	µA

*1 Except OSC0, TEST and $\overline{\text{RESET}}$
*2 OSC0, TEST and $\overline{\text{RESET}}$
*3 All input pins
*4 P1, P2
*5 P2
*6 P0, P1, P3
*7 $\overline{\text{RESET}}$, P0, P3
*8 TEST
*9 I_{REF} subtracted

A/D Converter Characteristics

(1) When f = 1 MHz

(V_{DD} = AV_{DD} = 5 V ± 10%, GND = AGND = 0 V, Ta = –40 to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the recommended circuit (Figure 1). Analog input source impedance RI ≤ 5 kΩ	—	—	8	bit
Linearity error	E_L		—	—	+1 –1	LSB
Differential linearity error	E_D		—	—	±0.5	LSB
Crosstalk	E_{CT}	Refer to the measuring circuit (Figure 2).	—	—	±0.5	LSB
Conversion time	t_{CONV}	f_{OSC}=1 MHz	—	60	—	µs/CH

(2) When f = 4.2 MHz

(V_{DD} = AV_{DD} = 5 V ± 10%, GND = AGND = 0 V, Ta = –40 to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the recommended circuit (Figure 1). Analog input source impedance RI ≤ 5 kΩ	—	—	8	bit
Linearity error	E_L		—	—	+1.5 –1.5	LSB
Differential linearity error	E_D		—	—	±0.5	LSB
Crosstalk	E_{CT}	Refer to the measuring circuit (Figure 2).	—	—	±0.5	LSB
Conversion time	t_{CONV}	f_{OSC}=4.2 MHz	—	14	—	µs/CH

Definition of Terms

Resolution Capacity

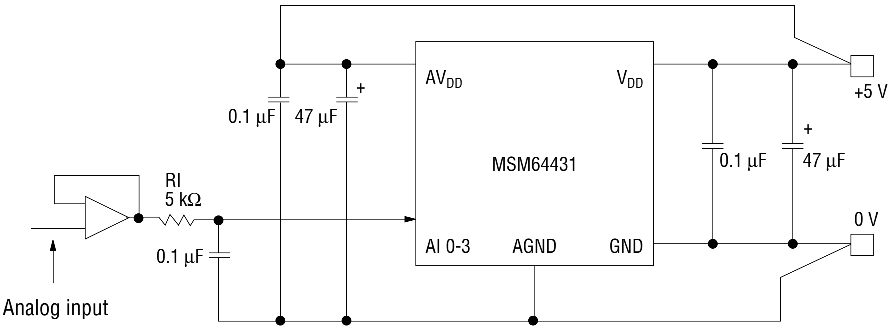
This refers to the minimum input analog value that is distinguishable. For 8 bits, 2^8=256 (AV_{DD} ∏256) can be resolved.

Linearity Error

This refers to the variance between the ideal characteristics of an 8-bit A/D converter and the actual conversion characteristics when no quantitized error is involved.
Ideal conversion characteristics refer to steps that divide the voltage between AV_{DD} and AGND into 256.

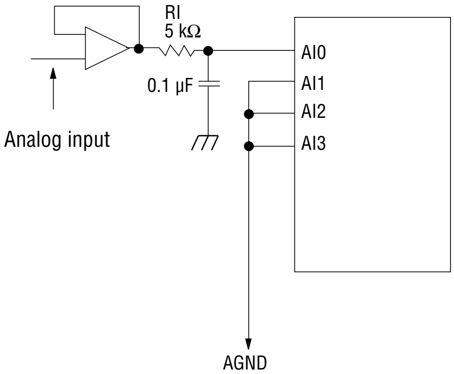
Differential Linearity Error

This refers to the smoothness of the conversion characteristics.
The width of analog input voltage corresponding to the variation of digital output for 1 bit is ideally 1LSB=AV_{DD} ∏256. The difference between this ideal bit size and a bit size at an arbitrary point in the conversion range is called differential linearity error.



RI (Analog input source impedance) ≤ 5 kΩ

Figure 1. Recommended circuit



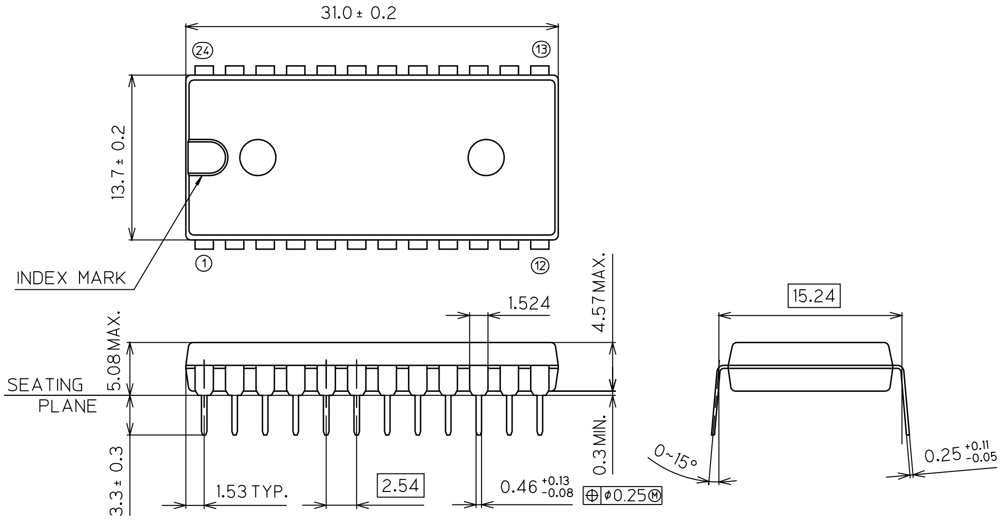
Analog input. The difference in the A/D conversion results between the identical analog input applied to AI 0-3 and the result by the left figure is taken to be caused by crosstalk.

Figure 2. Crosstalk measuring circuit

PACKAGE DIMENSIONS

(Unit : mm)

DIP24-P-600-2.54

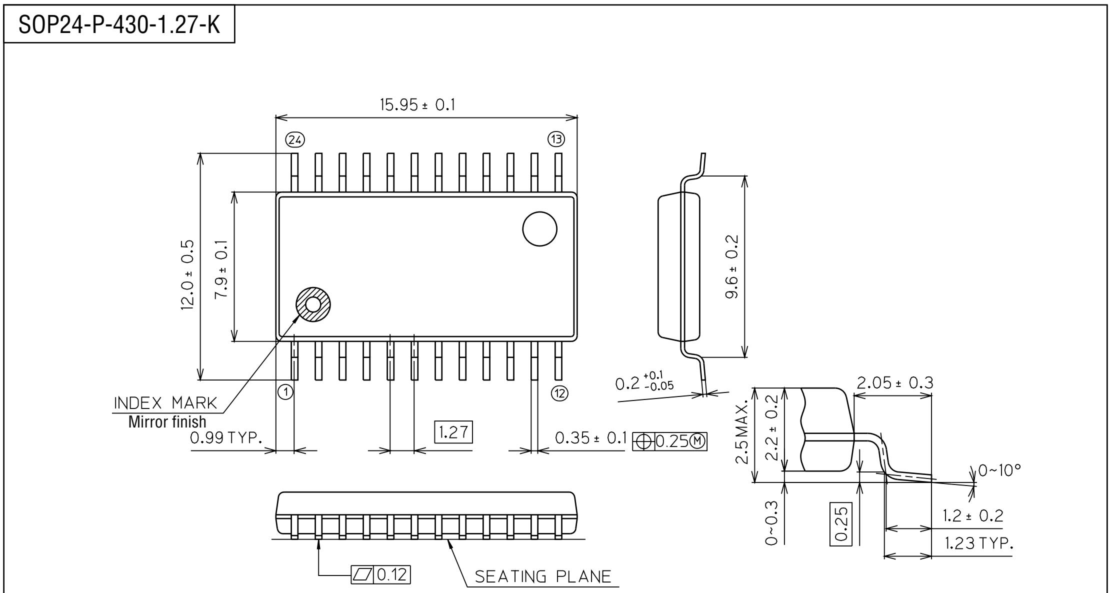


Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	3.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

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