OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM6889

Multi-Function Telecommunication LSI

GENERAL DESCRIPTION

The MSM6889 is best suited to be used as a signal transmitter/receiver LSI for a telemetering system that employs a no-ringing communication system.

The meter terminal of a telemetering system consists of this device, meter, NCU, and communication controller.

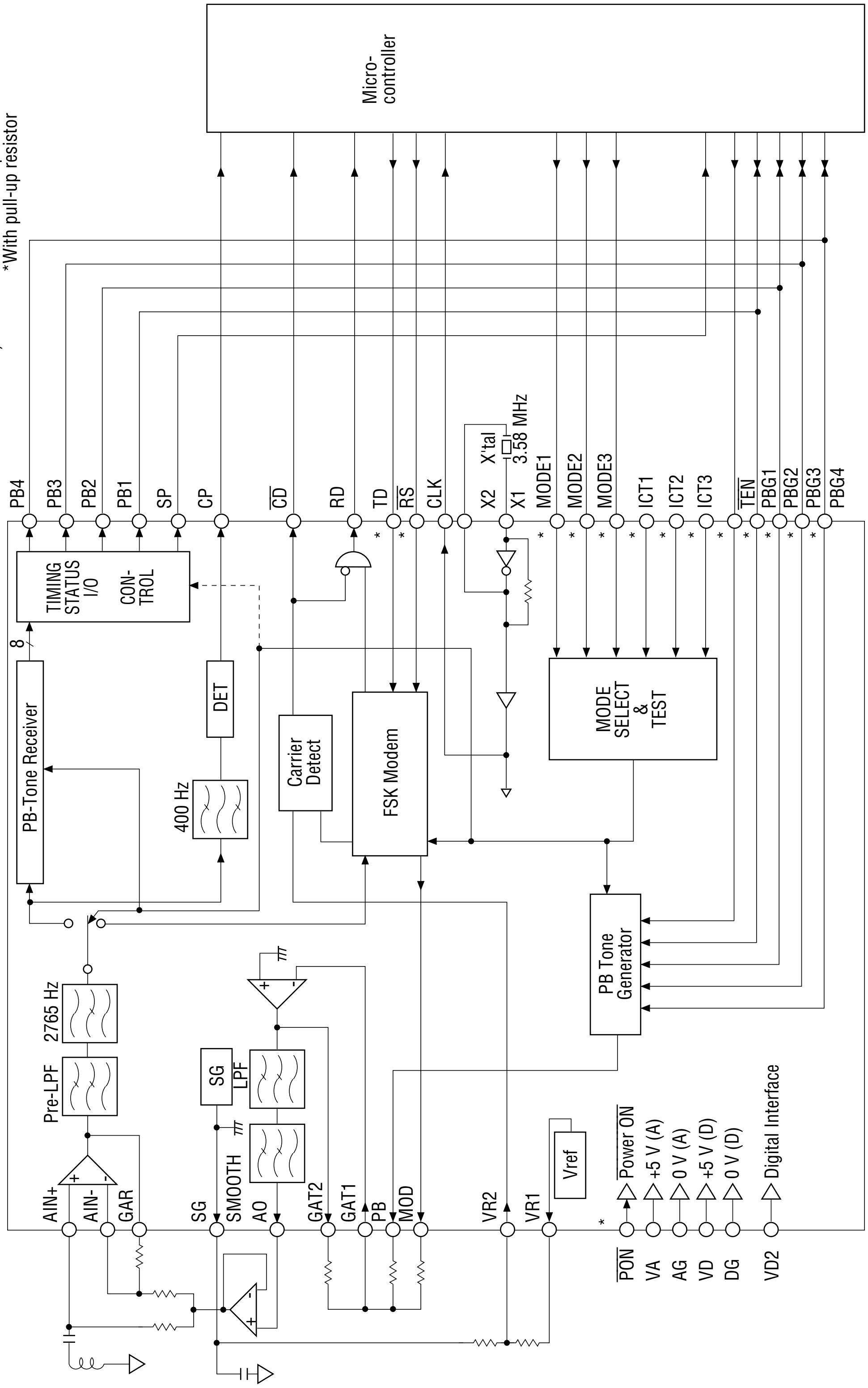
The MSM6889 contains a PB tone detector, a call progress tone (CPT) detector, a PB tone generator, and a 300-bps full-duplex modem conforming to ITU-T V.21.

FEATURES

- Power supply : +5 V ±10%, +2.5 V or higher for digital interface.
- Power consumption
  Operating mode : 9 mA Typ., 12 mA Max.
  Power down mode : 0.1 mA Max.
- The operating mode can be selected from PB tone transmit, PB tone detect, and FSK modem (answer/originate). The FSK modem cannot be operated concurrently with other functions. Modem test modes are also available.
- The call progress tone (CPT) detector operates in PB tone transmit mode or in FSK modem mode.
- PB receiver output is 3-state, and externally connectable to 4-bit input for PB tone generator through the bus line.
- Modem transmit/receive data, carrier detect, request to send, and call progress tone detect have their dedicated pins.
- Prefilter and smoothing filter are provided in analog input and output.
- On-chip 3.579545 MHz crystal oscillator
- 3.579545 MHz master clock output pin (CMOS compatible)
- Power down mode
- Modem : Conforms to ITU-T V.21 (300 bps, full-duplex)
- Transmit analog signals (modem signal, DTMF tone) : Level is independently adjustable externally. Carrier detect level is also adjustable externally.
- Package options:

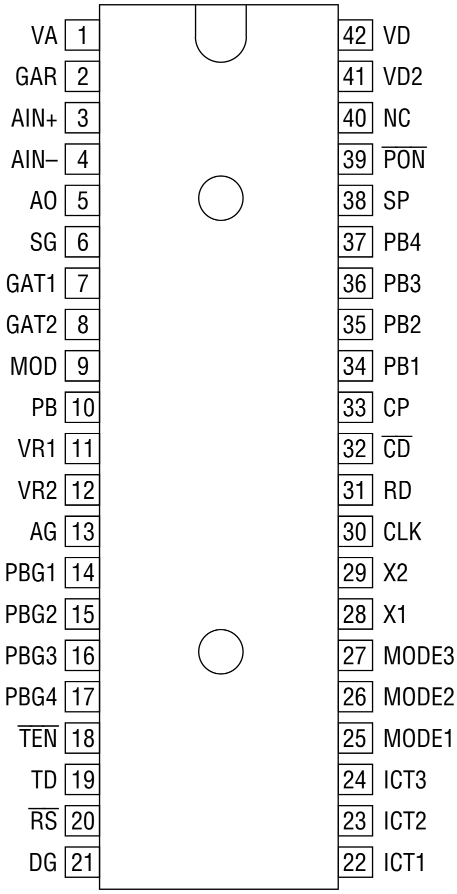
42-pin plastic DIP	(DIP42-P-600-2.54)	(Product name : MSM6889RS)
56-pin plastic QFP	(QFP56-P-1519-1.00-K)	(Product name : MSM6889GS–K)

BLOCK DIAGRAM



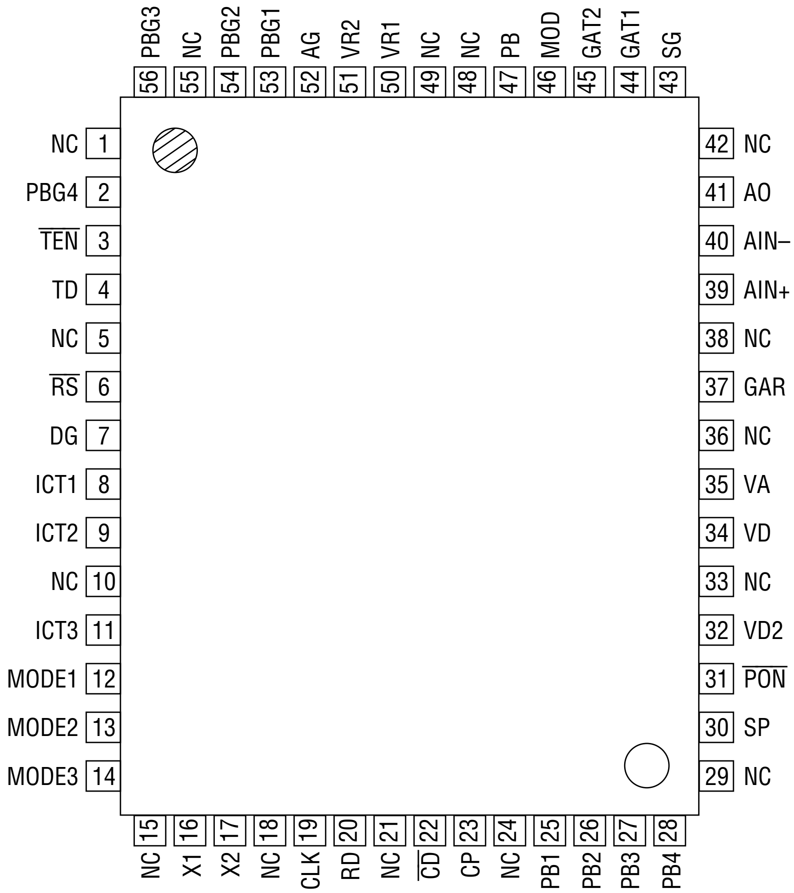
Note) PB1 to PB4: 3-State Outputs
*With pull-up resistor

PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

NC : No connect pin



56-Pin Plastic QFP

NC : No connect pin

PIN DESCRIPTION

Pin Number		Name	I/O	Description
RS	GS			
1	35	VA	—	+5 V Power Supply (Analog Circuit). When power is turned on or the power down mode is released, the device must be put into the PB tone transmit mode or PB tone detect mode.
2	37	GAR	O	Output, non-inverting input and inverting input pins of on-chip operational amplifier. No hybrid transformer is required by use of these pins. (See Fig. 2.)
3	39	AIN+	I	
4	40	AIN–	I	
5	41	AO	O	Analog signal output. PB tone or modem transmit signal is output from this pin.
6	43	SG	O	On-chip signal ground, having a potential of about +2.5 V.
7	44	GAT1	I	PB is the PB tone output and MOD is the modem signal output. By connecting external resistors to GAT1 and GAT2 pins, signal level can be set at required values for the modem signal and the PB tone that are output from AO, independently. (See Fig. 3.)
8	45	GAT2	O	
9	46	MOD	O	
10	47	PB	O	
11	50	VR1	O	These pins are used to externally adjust the received carrier detect(CD) signal level. The potential of VR1 to SG is about +1.1 V. The carrier detect level can be set at the required value by a on-chip resistor divider between VR1 and SG. The given potential to VR2 is set about +0.88 V with high resistance inside the IC. (See Fig. 4.)
12	51	VR2	I	
13	52	AG	—	Analog Ground, 0 V.
14	53	PBG1	I*	Inputs used to specify PB tone to be sent. PB1 to PB4 can be connected externally like 4-bit bus line. Data is latched at the falling edge of $\overline{\text{TEN}}$. (See Fig. 7 and Fig. 8.)
15	54	PBG2	I*	
16	56	PBG3	I*	
17	2	PBG4	I*	

* Digital input pulled up by a high resistance inside the IC.

Pin Number		Name	I/O	Description
RS	GS			
18	3	$\overline{\text{TEN}}$	I*	PB tone transmit enable. PBG1 to PBG4 data are latched at the falling edge of $\overline{\text{TEN}}$, and PB tone is generated at digital "0" level. (See Fig. 7.)
19	4	TD	I*	Modem transmit serial data input. Data stream less than 300 bps should be input. Digital "1" and "0" correspond to "Mark" and "Space" respectively.
20	6	$\overline{\text{RS}}$	I*	Request to send data input . While $\overline{\text{RS}}$ is at digital "0" level, modem transmit is enabled.
21	7	DG	—	Digital Ground, 0 V.
22	8	ICT1	I*	Input used to select call progress tone (CPT) detect output waveform. (See Fig. 9.)
23	9	ICT2	I*	Used to check performance characteristics of the IC. Independent of operating mode. Leave these pins open.
24	11	ICT3	I*	
25	12	MODE1	I*	Inputs used to specify operating mode. (See Table 1.)
26	13	MODE2	I*	
27	14	MODE3	I*	
28	16	X1	I	3.579545 MHz crystal resonator should be connected to X1 and X2. When applying external clock to the device, it should be connected to X2 through the AC coupling capacitor of 100 pF and X1 has to be open.
29	17	X2	O	
30	19	CLK	O	3.579545 MHz clock output.
31	20	RD	O	Modem receive serial data output. Digital "1" and "0" correspond to "Mark" and "Space" respectively. When $\overline{\text{CD}}$ (Carrier Detect) is off, RD is hold at "Mark" state.
32	22	$\overline{\text{CD}}$	O	Carrier Detect output. Digital "0" and "1" represent "Detect" and "No-detect" respectively.

* Digital input pulled up by a high resistance inside the IC.

Pin Number		Name	I/O	Description
RS	GS			
33	23	CP	O	Call progress tone (CPT) detect output. When a CPT is detected, the waveform selected by ICT1 is output. (See Fig. 9.)
34	25	PB1	O	Receive PB tone code outputs. The output impedance of these pins becomes high except when the device operates as PB tone receiver. (See Fig. 7 and Fig. 8.)
35	26	PB2	O	
36	27	PB3	O	
37	28	PB4	O	
38	30	SP	O	PB tone receive data present. Digital "1" represents that this pin is receiving the PB tone. (See Fig. 8.)
39	31	$\overline{PON}$	I	Power down mode select. Digital "1" on this pin puts the whole circuit of the device into the power down state.
40	—	NC	—	No connection.
41	32	VD2	—	Power supply for digital interface output. The supply voltage from +2.5 V to VD is possible for VD2. For example, when the device interfaces to the MCU working on +3 V supply, the +3 V supply has to be applied to the VD2 pin. Note that this function is effective to all of digital output pins except X1, X2, and CLK. There is no restriction regarding the power supplies (VD and VD2) applying procedure.
42	34	VD	—	+5 V power supply (digital circuit). When power is turned on or the power down mode is released, the device must be put into the PB tone transmit mode or PB tone detect mode.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VA, VD	Ta = 25°C with respect to AG and DG	–0.3 to 7	V
	VD2		–0.3 to VD	
Input Pin Voltage			–0.3 to VA(VD) + 0.3	
Storage Temperature		—	–65 to 150	°C
Pin Soldering Temperature		Within 10 sec	260	

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage		VA, VD	—	4.5	5.0	5.5	V
		VD2		2.5	—	VD	
Digital Input Voltage		V_{IH}	—	2.0	—	VD	V
		V_{IL}		0	—	0.8	
Digital Output Current		I_{OH}	When VD2 = VD (excluding) X2	–0.05	—	—	mA
		I_{OL}		—	—	0.4	
Operating Temperature		T_{op}	—	–40	—	+85	°C
Input Clock Frequency		f_{CLK}	—	–0.1	—	+0.1	%
Bypass Capacitance		VA	—	0.1 + 10	—	—	µF
		VD, VD2		1	—	—	
Crystal	Frequency Deviation		At 25°C ±5°C	–100	—	+100	ppm
	Temperature Characteristics		At –40°C to ±85°C	–50	—	+50	
	Equivalent Series Resistance		—	—	—	50	Ω
	Load Capacitance		—	—	16	—	pF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(VA, VD, VD2 = +5 V ±10%, Ta = –40°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current	I_{AD}	$I_A + I_D + I_{D2}$ (VD2 = VD)	$\overline{PON}$ = "0"	—	9	12	mA
	I_{PD}		$\overline{PON}$ = "1"	—	0.01	0.1	mA
Digital Input Current*	I_{IH}	VD2 = VD	$V_I = V_{IH}$ Max.	–10	—	10	μA
	I_{IL}		$V_I = V_{IL}$ Min.	–100	—	10	
Digital Output Voltage	V_{OH}		$I_O = I_{OH}$ Min.	2.4	—	VD2	V
	V_{OL}		$I_O = I_{OL}$ Max.	0	—	0.4	

* Internal pull-up resistor

Analog Interface and Dynamic Characteristics

(VD = VA = 5 V ±10%, Ta = –40°C to +85°C)

Parameter	Condition				Min.	Typ.	Max.	Unit
Modem Transmit Level	MOD	$R_L \geq 20$ kΩ "Mark" and "Space" Signals			–3	–1	+1	dBm
					1.55	1.95	2.46	V_{P-P}
PB Tone Send Level	PB	$R_L \geq 20$ kΩ	Low-Group Tone		–8.5	–6.5	–4.5	dBm
			High-Group Tone		–7.5	–5.5	–3.5	dBm
Output Voltage Swing	AO	$R_L \geq 20$ kΩ			2.2	3	—	Vp-p
Output Load Resistance	MOD, PB, GAT2, AO				20	—	—	kΩ
Signal Level Relative Value	MODEM	"Mark" & "Space" Signals			–2	0	2	dB
	PB Tone	High-Gr. Tone & Low-Gr. Tone			0	1	2	dB
Output DC Voltage	MOD, PB AO (When GAT1 and GAT2 are connected)				$\frac{VA}{2} - 0.1$	$\frac{VA}{2}$	$\frac{VA}{2} + 0.1$	V
Modem Transmit Carrier Frequency	Originate Mode	MARK	TD	"1"	976	980	984	Hz
		SPACE		"0"	1176	1180	1184	
	Answer Mode	MARK		"1"	1646	1650	1654	
		SPACE		"0"	1846	1850	1854	
Out-of-band Energy	4 to 8 kHz	P : In-band Signal Energy (0.3 kHz to 3.4 kHz) Measured at primary side of transformer line.			—	—	P-20	dB
	8 to 12 kHz				—	—	P-40	dB
	12 kHz to				—	—	P-60	dB
PB Tone Frequency	With respect to nominal frequency				–1.5	—	+1.5	%
PB Tone Distortion	Harmonics/Fundamental				—	—	–23	dB
PBG1 to PBG4 Input Data Setup Time	TPBGS, Fig. 7				250	—	—	ns
PBG1 to PBG4 Input Data Hold Time	TPBGH, Fig. 7				250	—	—	ns

Analog Interface and Dynamic Characteristics (Continued)

(VD = VA = 5 V ±10%, Ta = –40˚C to +85˚C)

Parameter	Condition		Min.	Typ.	Max.	Unit
Input Impedance	AIN+, 0 to 10 kHz		20	—	—	kΩ
Modem Receive Signal Level	AIN+, FSK Demodulator Signal		—	—	–6	dBm
Carrier Detect (CD) Signal Level	VR2; Open Answer mode: 1080 Hz Originate mode: 1750 Hz	OFF→ON	—	—	–42	dBm
		ON→OFF	–48	—	—	dBm
CD Level Hysteresis	Answer mode: 1080 Hz Originate mode: 1750 Hz		1	—	—	dB
CD Delay Time	–60 dBm → –20 dBm Step		10	—	40	ms
CD Hold Time	–20 dBm → –60 dBm Step		0	—	40	ms
Demod. Data Bias Distortion	300 bps, 1/0 Alternative Pattern		—	—	±10	%
NRTS Signal-to-Modem Receive Signal Ratio	vNRTS/v Receive Modem Signal NRTS: 2765 Hz ±30 Hz		—	—	–2	dB
CPT Detect Level	400 Hz		–40	—	–6	dBm
CPT Non-detect Level	400 Hz		—	—	–60	dBm
CPT Detect Frequency	R > 20% (square waves output) (See Fig. 9)		380	—	420	Hz
CPT Non-detect Frequency	R > 20% (square waves output) (See Fig. 9)		500	—	—	Hz
			—	—	300	
CPT Detect Delay Time	—		—	20	—	ms
CPT Detect Hold Time	—		—	20	—	ms
PB Tone Detect Amplitude	For Each Signal Tone		–46	—	–6	dBm
PB Tone Non-detect Amplitude	For Each Signal Tone		—	—	–60	dBm
Detect Frequency	With respect to Nominal Frequency		—	—	±1.5	%
Non-detect Frequency	With respect to Nominal Frequency		±3.8	—	—	%
Allowable twist	High-Gr. Tone/Low-Gr. Tone		–6	—	+6	dB
Allowable Noise Level	Noise (0.3 kHz to 3.4 kHz) Level/Tone Level		—	–12	—	dB
Dial Tone Rejection Ratio	380 Hz to 420 Hz		37	—	—	dB
Signal Repetition Time	T_C	Fig. 1	120	—	—	ms
Time to Receive	T_S		49	—	—	ms
Invalid Tone Duration	T_I		—	—	24	ms
Output Delay Time	T_G		24	39	49	ms
Interdigit Pause	T_P		30	—	—	ms
Acceptable Drop Out	T_B		—	—	2	ms
SP Delay Time	T_{SP}		6	8	10	ms
Output Trailing edge Delay	T_D		21	28	35	ms

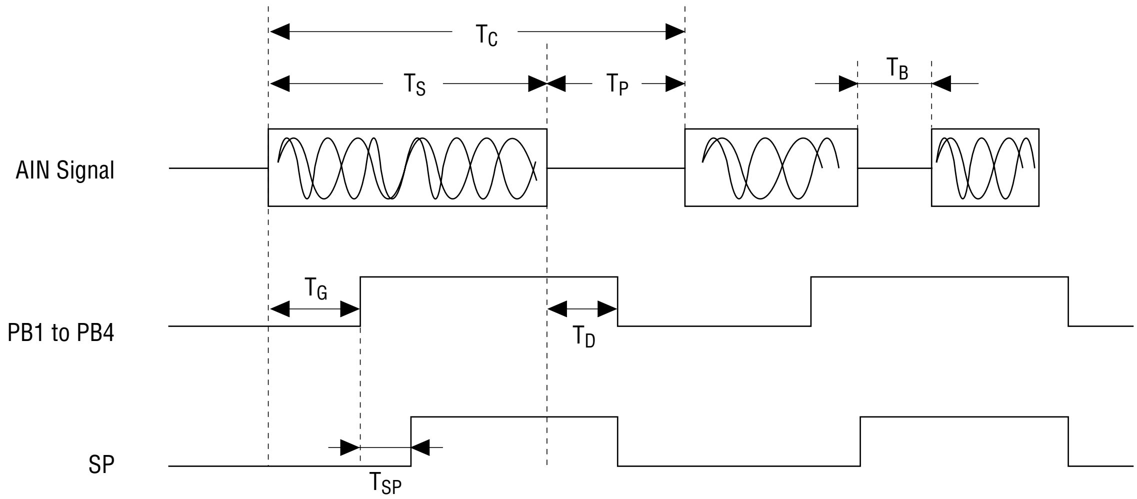


Figure 1

FUNCTIONAL DESCRIPTION AND APPLICATION

Resistance Hybrid Condition (Ideal Condition)

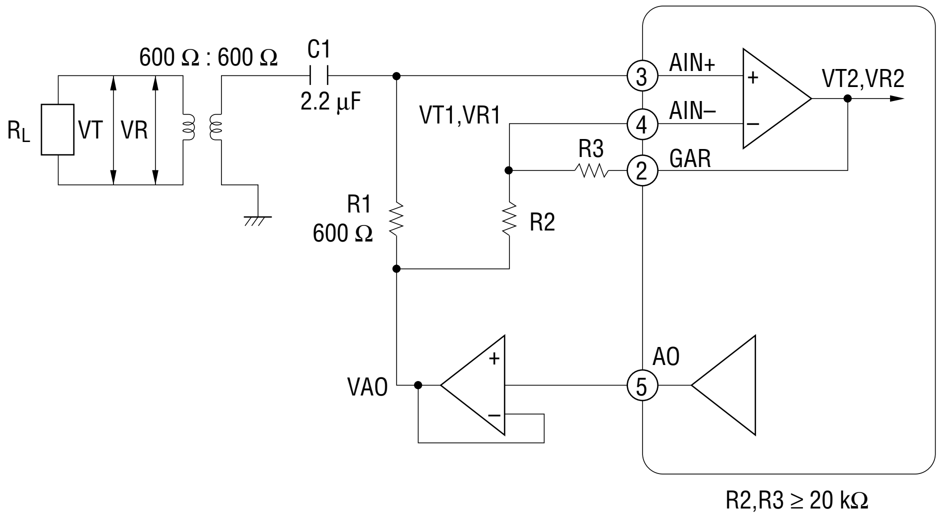


Figure 2

C1 is an ignorable impedance in the voice frequency band; therefore, if a line transformer and phone line impedance are ideal (R_L = 600 Ω pure resistance), the signal levels at each point are as shown below.

VT, VR	:	Transmit at 2W on phone line, receive signal level (balanced)
VT1, VR1	:	Transmit at pin 3 (AIN+), receive signal level (unbalanced)
VAO	:	Transmit signal level at pin 5 (AO) (unbalanced)
VT2	:	Leaking of transmit signal into receive circuit (unbalanced)
VR2	:	Receive signal level of the device (unbalanced)

1) VT = VT1 = 1/2 × VAO
The transmit signal level (voltage) on phone line is half the level at the output pin (AO) of the device. (600 Ω : a 600 Ω line transformer is used)

2) VR1 = VR

3) $$VT2 = VT1 \times \left(1+\frac{R3}{R2}\right) + VAO \times \left(-\frac{R3}{R2}\right)$$

$$= \frac{1}{2}VAO \times \left(1+\frac{R3}{R2}\right) - VAO \times \frac{R3}{R2} = \frac{1}{2}VAO \times \left(1-\frac{R3}{R2}\right)$$

Then, where R2 = R3 (e.g., 51 kΩ), VT2 = 0.
This means that the transmit signal is no longer leaking into the receive circuit.

4) $VR2 = VR1 \times \left(1+\frac{R3}{R2}\right)$, where R2 = R3, $VR2 = 2 \times VR1 = 2 \times VR$

Setup of Transmit Signal Levels

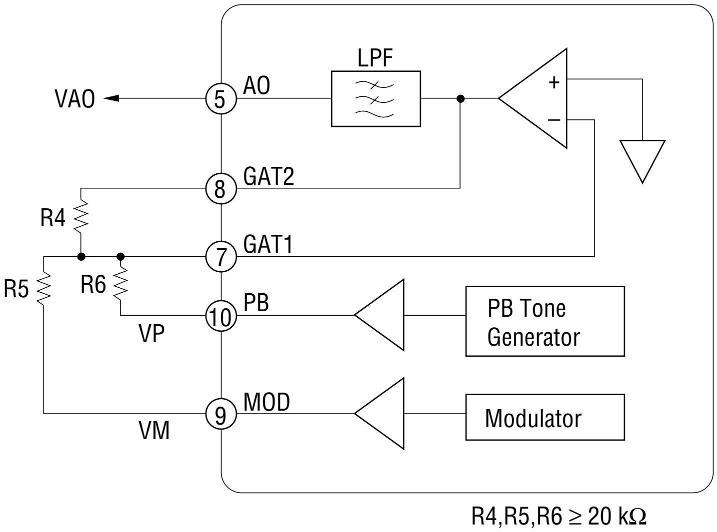


Figure 3

The modulation analog signal and PB tone from the modem are not sent at a time. The signal to be sent is determined by the operating mode specified.
This device is provided with the pins for specifying levels of these transmit signals independently. The answer tones, which are generated from MODULATOR, are handled as modem signals.

VM : Modem signal level (voltage) at MOD (pin 9)
VP : PB tone level (voltage) at PB (pin 10)

When the external resistors are R4, R5 and R6, the signal levels at AO (pin 5) are as shown below.

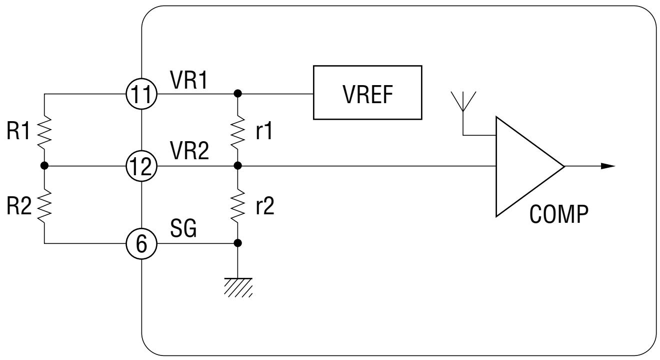
$$\text{VAO (modem)} = \frac{R4}{R5} \times VM$$

$$\text{VAO (PB)} = \frac{R4}{R6} \times VP$$

Note : R4, R5, R6 ≥ 20 kΩ

As described in "Resistance Hybrid Condition", signal levels actually sent over a phone line will be half the above mentioned values under the ideal condition.

External Setup of Carrier Detect Level



R1//r1 + R2//r2 ≥ 20 kΩ

r1: 250 kΩ, r2 : 1 MΩ

Figure 4

Operating Mode

Table 1 Operating Mode Table

Mode Select 1	Mode Select 2	Mode Select 3	Operating Mode		PB GEN.	PB REC.	FSK MODEM	CPT REC. ICT1 = "1"	CPT REC. ICT1 = "0"
0	0	0	PB Tone Transmit		*				*
1	0	0	PB Tone Detect			*			
0	1	0	Originate Mode Modem (O)				*	*	
1	1	0	Answer Mode Modem (A)				*	*	
0	0	1	Analog Loop Back Test (ALB)	O			*	*	
1	0	1		A			*	*	
0	1	1	Remote Digtal Loop Back Test (RDLB)	O			*	*	
1	1	1		A			*	*	

* : Active
When power is turned on or the power down mode is released, put the device into the PB tone transmit mode or PB tone detect mode.

Signal flow concept for the modem normal operating mode is shown in Fig. 5.

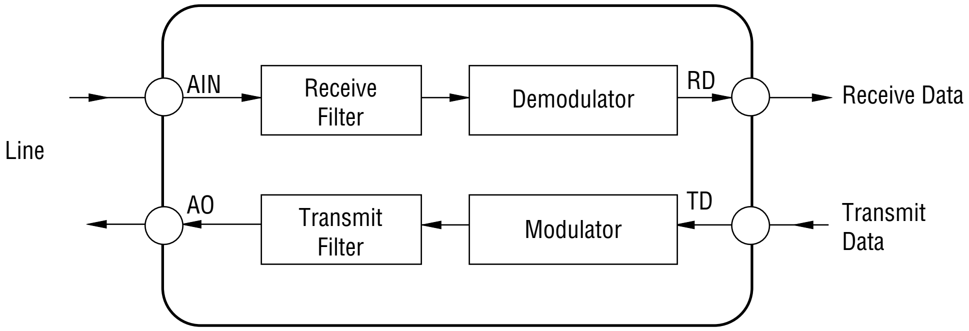


Figure 5

In the test modes, signal flow shown in Fig. 6 is used. O/(originate)/A(answer) in the test mode is the expression where the modulator side is referred to as the basis.

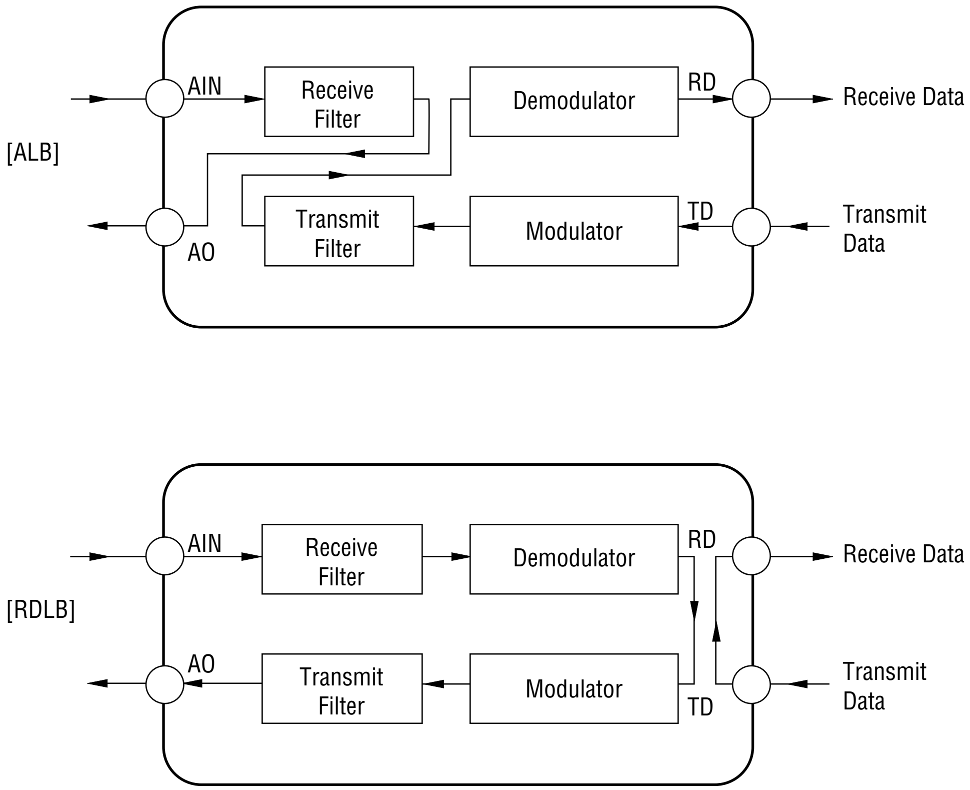


Figure 6

PB Tone Transmit Mode and PB Tone Detect Mode

When PBG1 to PBG4 are externally connected to PB1 to PB4 so as to use them as 4-bit bus lines, their tone generation timings are as shown below.

1) PB Tone Transmit Mode

When $\overline{TEN}$ is in the digital "0" state, PB tone is generated according to Table 2.

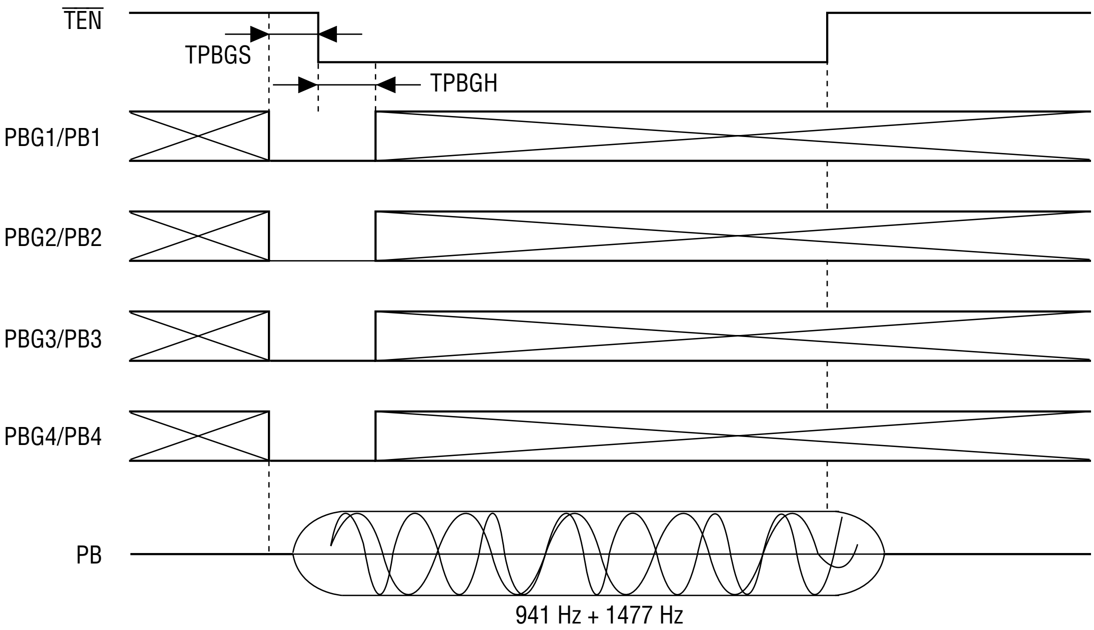


Figure 7

2) PB Tone Detect Mode

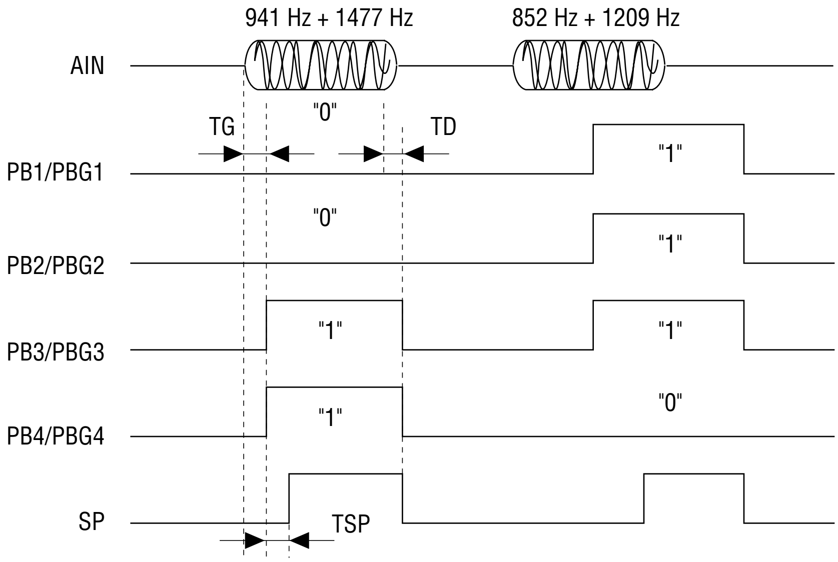


Figure 8

Table 2 PB Tone Code Table

Button	Low-Group Freq. (Hz)				High-Group Freq. (Hz)				PB4/	PB3/	PB2/	PB1/
	697	770	852	941	1209	1336	1477	1633	PBG4	PBG3	PBG2	PBG1
1	*				*				0	0	0	1
2	*					*			0	0	1	0
3	*						*		0	0	1	1
4		*			*				0	1	0	0
5		*				*			0	1	0	1
6		*					*		0	1	1	0
7			*		*				0	1	1	1
8			*			*			1	0	0	0
9			*				*		1	0	0	1
0				*		*			1	0	1	0
*				*	*				1	0	1	1
#				*			*		1	1	0	0
A	*							*	1	1	0	1
B		*						*	1	1	1	0
C			*					*	1	1	1	1
D				*				*	0	0	0	0

Call Progress Tone (CPT) Detect Mode

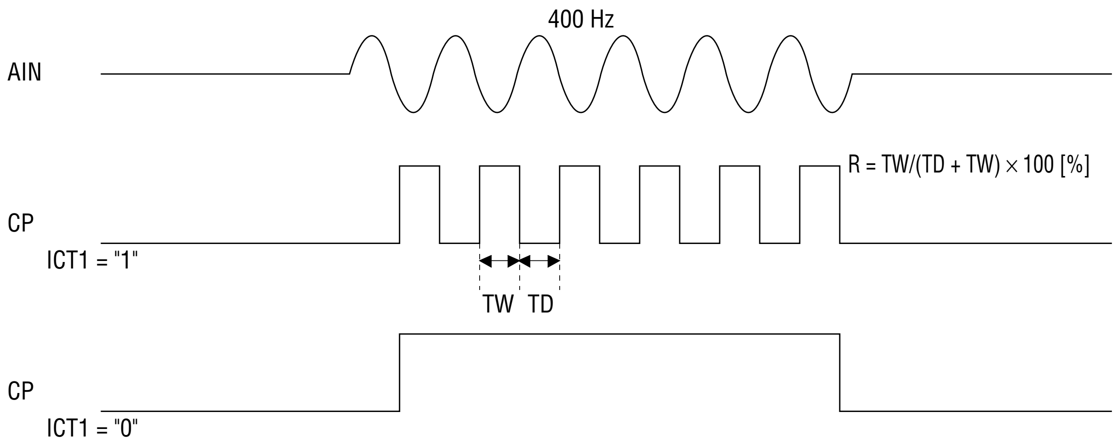
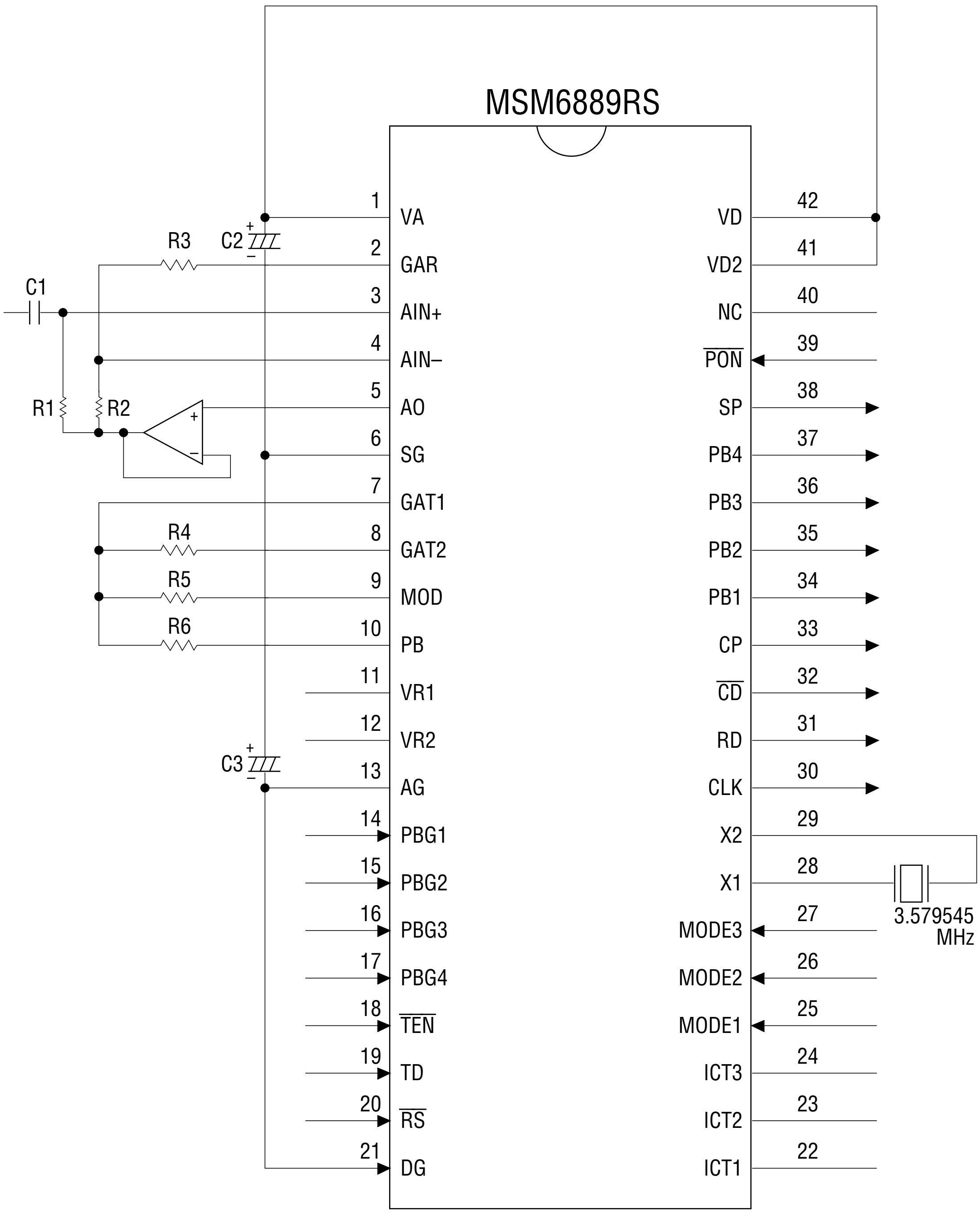


Figure 9

APPLICATION CIRCUIT

Pin Connection



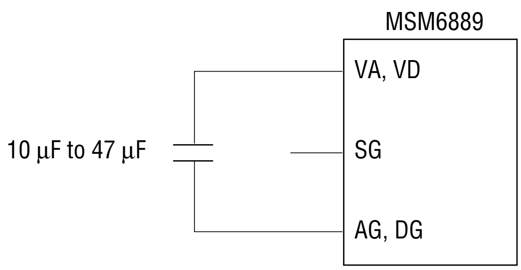
R1 = 600 Ω, R2 = R3 = R4 = R5 = R6 = 51 kΩ
C1 = 2 μF, C2 = C3 = 10 μF

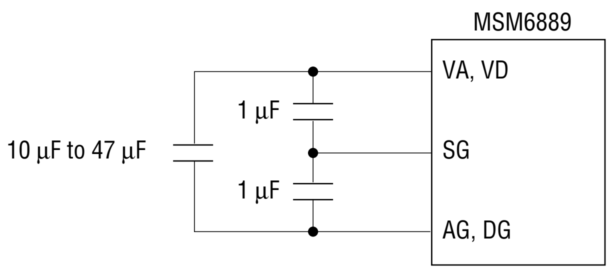
Bypass Capacitor Connections

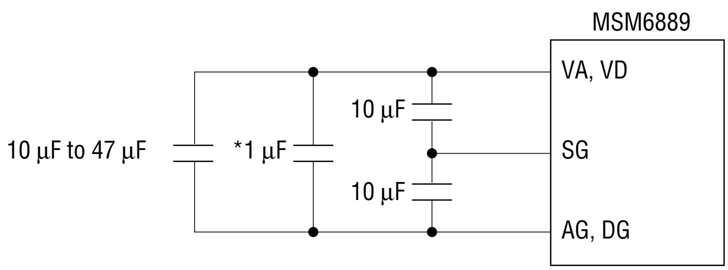
The MSM6889 contains analog circuits.

Note that noise occurred in the power supply by trouble in other circuits may cause degradation in characteristics of the device.

The examples of connected bypass capacitors of the MSM6889 are shown below.





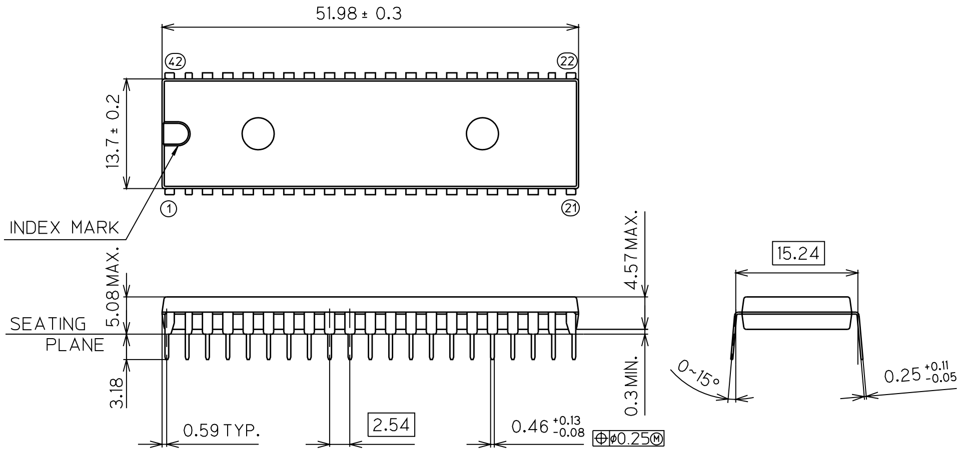


* Laminated ceramic capacitor

PACKAGE DIMENSIONS

(Unit : mm)

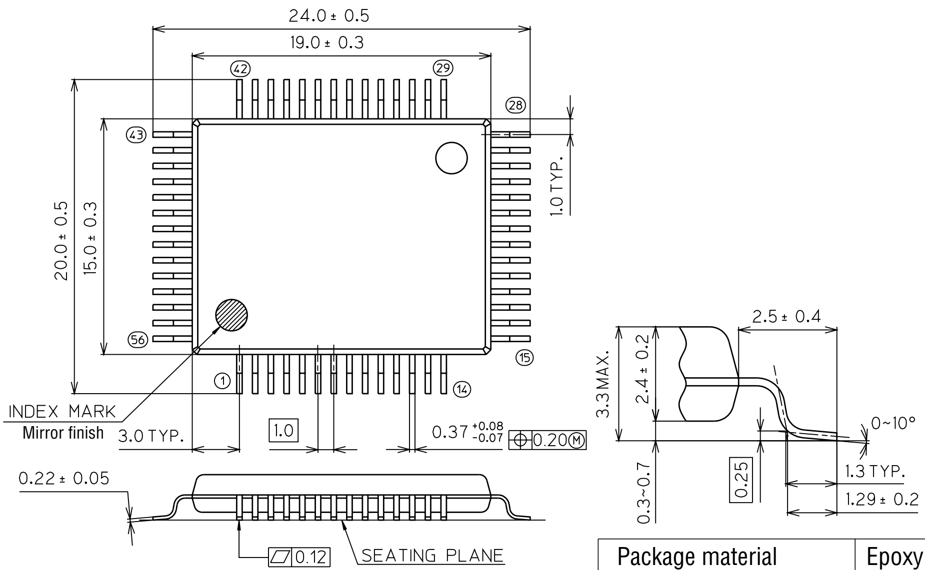
DIP42-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.20 TYP.

(Unit : mm)

QFP56-P-1519-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	1.46 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).