

**OKI**

**MSM9552/9553**  
**IC for FM Multiplex**  
**Broadcast Reception**  
**User's Manual**

**Ver. 1.0**

ISSUE DATE: Mar., 1998

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# *Chapter 1*

## GENERAL DESCRIPTION

## 1. GENERAL DESCRIPTION

The MSM9552 and MSM9553 are LSI devices which demodulate FM character multiplex signals in the DARC (Data Radio Channel) format to acquire digital data. These devices operate on 5 V and 3 V, respectively. In the DARC format, baseband signals at ordinary FM broadcasting frequencies are multiplexed with 16 kbps digital data which are L-MSK-modulated at 76 kHz.

Each device has a bandpass filter consisting of SCF, frame synchronization circuit, and error correction circuit, on a single chip.

They allow a system for acquisition of digital data to be easily constructed by externally mounting an FM receiver tuner, microcontroller for control, and memory for temporary storage of data.

The MSM9552 and MSM9553 have a simple configuration, and are equipped with only necessary functions. By making changes to software for the external microcontroller, the MSM9552 and MSM9553 meet the various requirements of FM multiplex broadcasting services to be offered in future.

These devices are best suited for radio sets and information devices using FM character multiplex broadcasting, which began in Japan in October 1994. The MSM9553 is especially suitable for portable units.

### Features

- Built-in Bandpass Filter (SCF)
- Built-in Block Synchronization Circuit and Frame Synchronization Circuit
- Setting of Synchronization Protecting Stage number
- Regeneration of Data Clocks by Digital PLL
- 1T Delay Detection
- Built-in Error Correcting Circuit
- Built-in Layer 4 and Layer 2 CRC Processing Circuit
- International Frame Formats A (supporting a real time block), B, and C available
- Microcontroller Parallel Interface
- Clock Output for External Devices (64 kHz to 8.192 MHz selectable)
- Power Source: 5 V (MSM9552), 3 V (MSM9553)
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM9552GS-2K, MSM9553GS-2K)





## *Chapter 2*

# BLOCK DIAGRAM

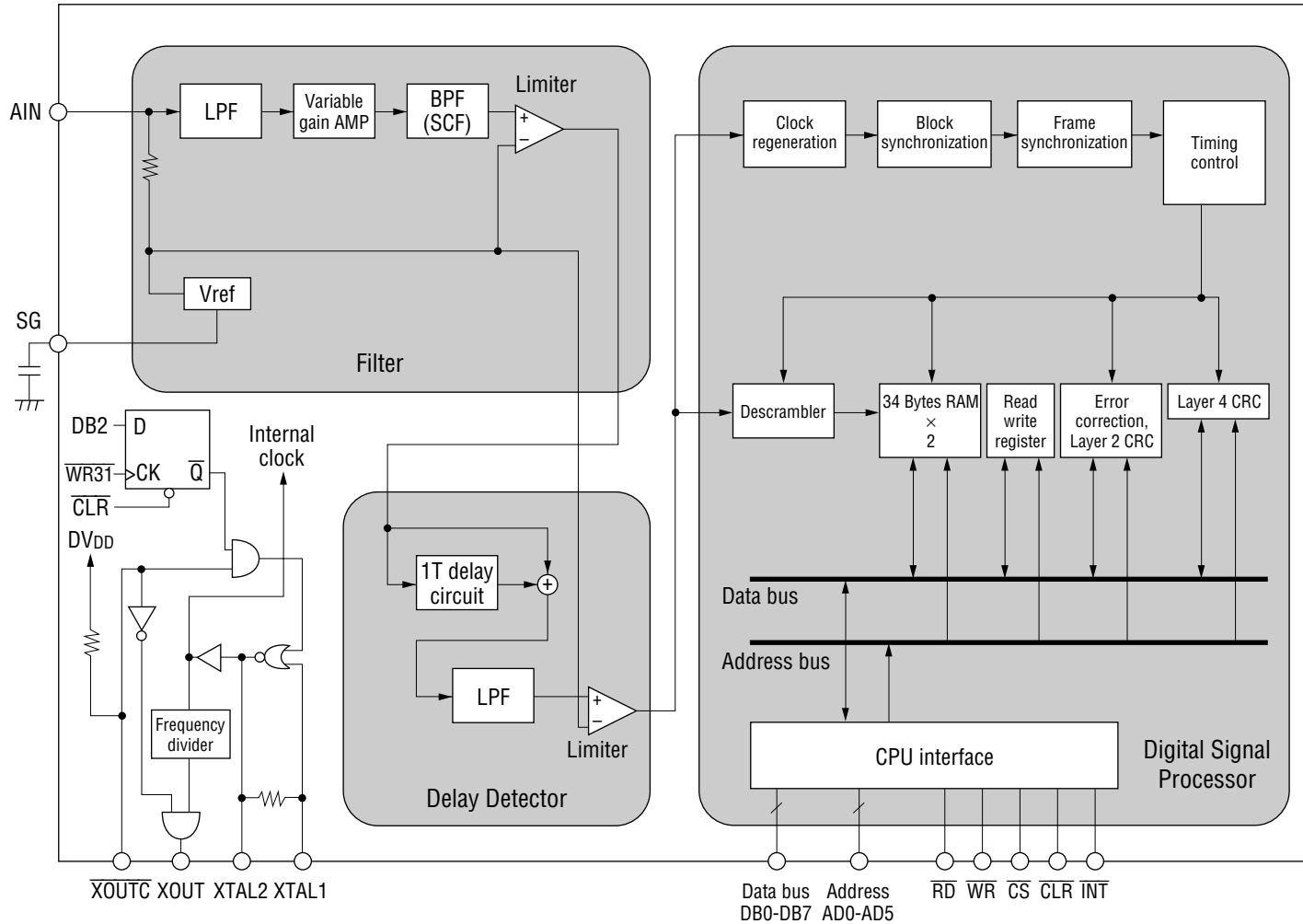


Figure 2.1 Block Diagram



## ***Chapter 3***

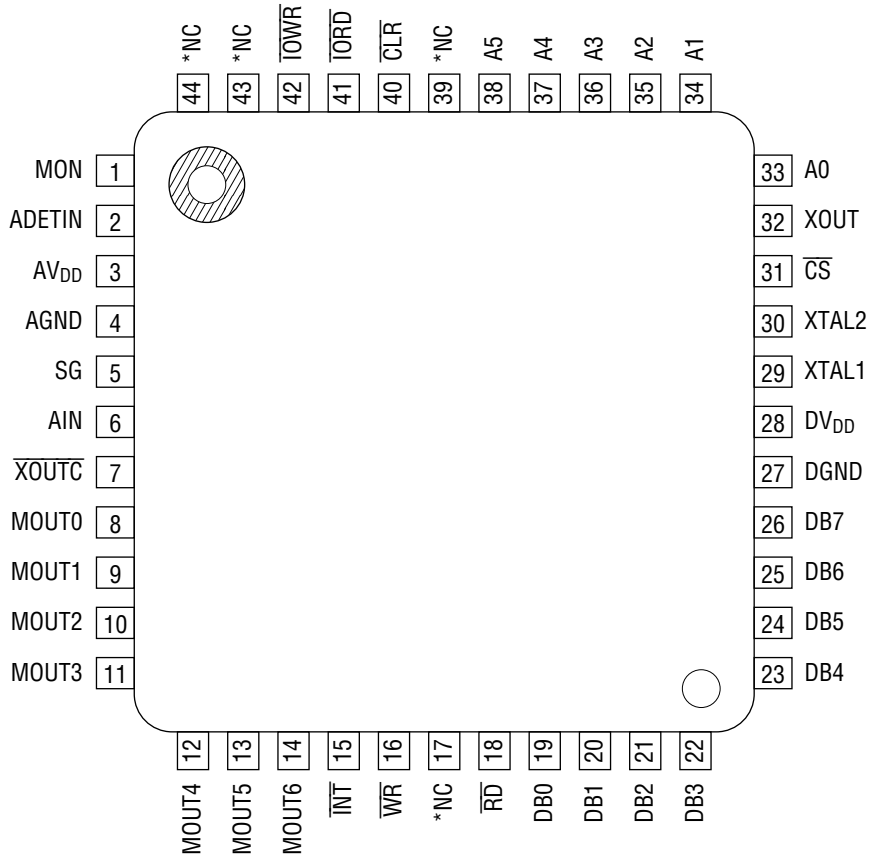
# **PIN INFORMATION**

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### 3. PIN INFORMATION

#### 3.1 PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

**Figure 3.1 Pin Layout**

\* Leave the NC pins (17, 39, 43, and 44) open.

### 3.2 PIN DESCRIPTIONS

**Table 3.1 Pin Description**

| Function                  | Symbol             | Pin   | Type | Description  |
|---------------------------|--------------------|-------|------|--|
| Microcontroller interface | $\overline{WR}$    | 16    | I    | Write signal to internal register.   |
|                           | $\overline{RD}$    | 18    | I    | Read signal to internal register.  |
|                           | $\overline{INT}$   | 15    | O    | Interrupt signal to microcontroller. When set to "L", an interrupt is generated.   |
|                           | $\overline{CS}$    | 31    | I    | Chip select signal. When set to "L", the read, write, and data bus signals become effective.   |
|                           | $\overline{CLR}$   | 40    | I    | When set to "L", the internal register is initialized, and the IC enters power down mode.  |
|                           | A0-A5              | 33-38 | I    | Address signal to internal register.   |
|                           | DB0-DB7            | 19-26 | I/O  | Data bus signal to internal register.  |
| Tuner interface           | AIN                | 6     | I    | FM multiple signal input.  |
|                           | SG                 | 5     | O    | Analog reference voltage pin. Connect a capacitor between this pin and the analog ground pin to prevent noise.                                     |
| Analog section test       | MON                | 1     | O    | Analog section waveform monitoring pin. The mode setting for the blocks in the analog section is specified by the analog section control register. |
|                           | ADETIN             | 2     | I    | Analog signal input pin for testing.   |
| Digital section test      | $\overline{TORD}$  | 41,   | I    | Digital section test signal input pins (pulled up internally).   |
|                           | $\overline{TOWR}$  | 42    | I    |  |
|                           | MOUT0-MOUT6        | 8-14  | O    | Digital section test signal and monitor output pins.   |
| Clock                     | XTAL1              | 29    | I    | 8.192 MHz crystal connection.  |
|                           | XTAL2              | 30    | O    | 8.192 MHz crystal connection.  |
|                           | XOUT               | 32    | O    | Pin to supply variable clock (64 kHz to 8.192 MHz) to external devices.  |
|                           | $\overline{XOUTC}$ | 7     | I    | XOUT control. "L" sets XOUT output, "H" sets XOUT output inhibit. This pin is pulled up internally.  |
| Power supply              | AV <sub>DD</sub>   | 3     | —    | Analog power supply.   |
|                           | AGND               | 4     | —    | Analog ground.   |
|                           | DV <sub>DD</sub>   | 28    | —    | Digital power supply.  |
|                           | DGND               | 27    | —    | Digital ground.  |

## ***Chapter 4***

# **ELECTRICAL CHARACTERISTICS**

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## 4. ELECTRICAL CHARACTERISTICS

### 4.1 MSM9552 ELECTRICAL CHARACTERISTICS

#### 4.1.1 Absolute Maximum Ratings

| No. | Parameter                 | Symbol    | Condition                                       | Rating                  | Unit             |
|-----|---------------------------|-----------|---|-------------------------|------------------|
| 1   | Power supply voltage      | $AV_{DD}$ | $AV_{DD} = DV_{DD}$<br>$T_a = 25^\circ\text{C}$ | -0.3 to +7.0            | V                |
|     |                           | $DV_{DD}$ |   |                         |                  |
| 2   | Input voltage             | $V_I$     |   | -0.3 to $AV_{DD} + 0.3$ |                  |
|     | Output voltage            | $V_O$     |   | -0.3 to $DV_{DD} + 0.3$ |                  |
| 3   | Maximum power dissipation | $P_D$     | $T_a = 25^\circ\text{C}$ , per package          | 400                     | mW               |
|     |                           |           | $T_a = 25^\circ\text{C}$ , per output           | 50                      |                  |
| 4   | Storage temperature       | $T_{STG}$ | —   | -55 to +150             | $^\circ\text{C}$ |

#### 4.1.2 Recommended Operating Conditions

| No. | Parameter                         | Symbol     | Condition                                   | Range                   | Unit             | Applied Pin     |
|-----|-----------------------------------|------------|---|-------------------------|------------------|-----------------|
| 1   | Power supply voltage              | $AV_{DD}$  | $AV_{DD} = DV_{DD}$                         | 4.5 to 5.5              | V                | $AV_{DD}$       |
|     |                                   | $DV_{DD}$  |   |                         |                  | $DV_{DD}$       |
| 2   | Crystal oscillation frequency     | $f_{XTAL}$ | —   | 8.192 MHz $\pm$ 100 ppm | —                | XTAL1,<br>XTAL2 |
| 3   | FM multiplex signal input voltage | $V_{AIN}$  | Composite signal including multiplex signal | 0.5 to 2*               | $V_{P-P}$        | AIN             |
| 4   | Operating temperature             | $T_a$      | —   | -40 to +85              | $^\circ\text{C}$ | —               |

\* The gain of the variable gain amplifier (VGain):  $\times 1$ ,  $\times 1.5$ ,  $\times 2$ , or  $\times 3$ .

The VGain should be adjusted to satisfy the equation:  $V_{AIN} \times \text{VGain} = 1.5 \text{ V to } 2.0 \text{ V}$ .



### 4.1.3 DC Characteristics

( $DV_{DD} = AV_{DD} = 5\text{ V} \pm 10\%$ ,  $DGND = AGND = 0\text{ V}$ ,  $T_a = -40\text{ to }+85^\circ\text{C}$ )

| No. | Parameter                  | Symbol     | Condition   | Min.                 | Typ. | Max.                 | Unit          | Applied Pin   |
|-----|----------------------------|------------|---|----------------------|------|----------------------|---------------|---|
| 1   | Input voltage              | $V_{IH}$   | —   | $0.8 \times DV_{DD}$ | —    | —                    | V             | $\overline{WR}$ , $\overline{RD}$ ,<br>$\overline{XOUTC}$ ,<br>DB0 to DB7,<br>XTAL1, $\overline{CS}$ ,<br>A0 to A5, $\overline{CLR}$ ,<br>$\overline{IORD}$ , $\overline{IOWR}$ |
|     |                            | $V_{IL}$   |   | —                    | —    | $0.2 \times DV_{DD}$ |               |   |
| 2   | Output voltage             | $V_{OH}$   | $I_{OH} = -1\text{ mA}$                             | $DV_{DD}$<br>-0.5    | —    | —                    | V             | MOUT0 to<br>MOUT6, $\overline{INT}$ ,<br>DB0 to DB7,<br>XOUT  |
|     |                            | $V_{OL}$   | $I_{OL} = 2\text{ mA}$                              | —                    | —    | 0.45                 |               |   |
| 3   | Input current 1            | $I_{IH1}$  | $V_{IH} = DV_{DD}$                                  | —                    | —    | 2                    | $\mu\text{A}$ | $\overline{WR}$ , $\overline{RD}$ , $\overline{CS}$ ,<br>DB0 to DB7,<br>A0 to A5,<br>$\overline{CLR}$   |
|     |                            | $I_{IL1}$  | $V_{IL} = DGND$                                     | -2                   | —    | —                    |               |   |
| 4   | Input current 2            | $I_{IH2}$  | $V_{IH} = AV_{DD}$                                  | —                    | —    | 2                    | $\mu\text{A}$ | ADETIN  |
|     |                            | $I_{IL2}$  | $V_{IL} = AGND$                                     | -2                   | —    | —                    |               |   |
| 5   | Input current 3            | $I_{IH3}$  | $V_{IH} = DV_{DD}$                                  | —                    | —    | 2                    | $\mu\text{A}$ | $\overline{XOUTC}$ ,<br>$\overline{IORD}$ , $\overline{IOWR}$   |
| 6   | Pull-up current            | $I_{pull}$ | $DV_{DD} = 5\text{ V}$ ,<br>$V_{IL} = DGND$         | 8                    | 35   | 110                  | $\mu\text{A}$ |   |
| 7   | Output off-leakage current | $I_{OH}$   | $V_{OH} = AV_{DD}$<br>During nonmonitoring (Hiz)    | —                    | —    | 2                    | $\mu\text{A}$ | MON   |
|     |                            | $I_{OL}$   | $V_{OL} = AGND$<br>During nonmonitoring (Hiz)       | -2                   | —    | —                    |               |   |
| 8   | Supply current             | $I_{DD}$   | During operation, no load<br>$f = 8.192\text{ MHz}$ | —                    | 16   | 32                   | mA            | $AV_{DD}$ , $DV_{DD}$   |
|     |                            |            | During power down,<br>no load                       | —                    | —    | 20                   | $\mu\text{A}$ |   |

#### 4.1.4 AC Characteristics

| No. | Parameter  | Symbol*       | Condition  | Min. | Typ. | Max. | Unit    | Applied Pin  |
|-----|--|---------------|--|------|------|------|---------|--|
| 1   | Write setup time                                       | $t_{SWR1}$    | —  | 10   | —    | —    | ns      | $\overline{WR}$ , $\overline{CS}$ ,<br>A0 to A5,<br>DB0 to DB7 |
|     |  | $t_{SWR2}$    | —  | 60   | —    | —    |         |  |
| 2   | Write hold time  | $t_{HWR}$     | —  | 10   | —    | —    | ns      | $\overline{WR}$ , $\overline{CS}$ ,<br>A0 to A5,<br>DB0 to DB7 |
| 3   | Write pulse width                                      | $t_{WWR}$     | —  | 65   | —    | —    | ns      | $\overline{WR}$  |
| 4   | Read setup time  | $t_{SRD}$     | —  | 10   | —    | —    | ns      | $\overline{RD}$ , $\overline{CS}$ ,<br>A0 to A5                |
| 5   | Read hold time   | $t_{HRD}$     | —  | 10   | —    | —    | ns      | $\overline{RD}$ , $\overline{CS}$ ,<br>A0 to A5                |
| 6   | Read pulse width                                       | $t_{WRD}$     | —  | 105  | —    | —    | ns      | $\overline{RD}$  |
| 7   | Interval between error correction data write and write | $t_{IWRWRE}$  | Error correction                                 | 250  | —    | —    | ns      | $\overline{WR}$  |
| 8   | Interval between error correction data read and read   | $t_{IRDRDE}$  | Error correction                                 | 250  | —    | —    | ns      | $\overline{RD}$  |
| 9   | Interval between error correction data write and read  | $t_{IWRRDE}$  | Error correction                                 | 100  | —    | —    | ns      | $\overline{WR}$ ,<br>$\overline{RD}$                           |
| 10  | Interval between layer 4 data clear and write          | $t_{ICLRWR4}$ | Layer 4 CRC                                      | 100  | —    | —    | ns      | $\overline{WR}$  |
| 11  | Interval between layer 4 data write and write          | $t_{IWRWR4}$  | Layer 4 CRC                                      | 4.5  | —    | —    | $\mu s$ | $\overline{WR}$  |
| 12  | Interval between layer 4 data write and read           | $t_{IWRRD4}$  | Layer 4 CRC                                      | 4.5  | —    | —    | $\mu s$ | $\overline{WR}$ ,<br>$\overline{RD}$                           |
| 13  | Read data output delay (1)                             | $t_{DRD1}$    | —  | —    | —    | 95   | ns      | $\overline{RD}$ ,<br>DB0 to DB7                                |
| 14  | Read data output delay (2)                             | $t_{DRD2}$    | —  | —    | —    | 80   | ns      | $\overline{RD}$ ,<br>DB0 to DB7                                |
| 15  | Interrupt CLR delay                                    | $t_{DINTCLR}$ | Step out interrupt<br>Error correction interrupt | 250  | —    | —    | ns      | $\overline{INT}$ ,<br>$\overline{WR}$                          |
| 16  | Error correction time (Horizontal direction)           | $t_{ERRL}$    | —  | —    | —    | 274  | $\mu s$ | $\overline{INT}$ ,<br>DB0                                      |
| 17  | Error correction time (Vertical direction)             | $t_{ERRV}$    | —  | —    | —    | 2178 | $\mu s$ | $\overline{INT}$ ,<br>DB0                                      |
| 18  | CLR pulse width  | $t_{WCLR}$    | —  | 200  | —    | —    | ns      | $\overline{CLR}$   |

\* See section 4.3, "TIMING DIAGRAM".

#### 4.1.5 Filter Characteristics

| No. | Parameter                      | Symbol | Condition   | Min. | Typ. | Max. | Unit | Applied Pin |
|-----|--------------------------------|--------|---|------|------|------|------|-------------|
| 1   | BPF pass band attenuation      | GAIN1  | 72 to 80 kHz<br>Variable gain amplifier<br>gain: 0 dB   | —    | —    | 3.0  | dB   | MON         |
| 2   | BPF block band attenuation (1) | GAIN2  | 0 to 53 kHz<br>Variable gain amplifier<br>gain: 0 dB    | 50   | —    | —    | dB   | MON         |
| 3   | BPF block band attenuation (2) | GAIN3  | 100 to 500 kHz<br>Variable gain amplifier<br>gain: 0 dB | 50   | —    | —    | dB   | MON         |

## 4.2 MSM9553 ELECTRICAL CHARACTERISTICS

### 4.2.1 Absolute Maximum Ratings

| No. | Parameter                 | Symbol    | Condition   | Rating                  | Unit               |
|-----|---------------------------|-----------|---|-------------------------|--------------------|
| 1   | Power supply voltage      | $AV_{DD}$ | $AV_{DD} = DV_{DD}$<br>$T_a = 25^{\circ}\text{C}$ | -0.3 to +7.0            | V                  |
|     |                           | $DV_{DD}$ |   |                         |                    |
| 2   | Input voltage             | $V_I$     |   | -0.3 to $AV_{DD} + 0.3$ |                    |
|     | Output voltage            | $V_O$     |   | -0.3 to $DV_{DD} + 0.3$ |                    |
| 3   | Maximum power dissipation | $P_D$     | $T_a = 25^{\circ}\text{C}$ , per package          | 400                     | mW                 |
|     |                           |           | $T_a = 25^{\circ}\text{C}$ , per output           | 50                      |                    |
| 4   | Storage temperature       | $T_{STG}$ | —   | -55 to +150             | $^{\circ}\text{C}$ |

### 4.2.2 Recommended Operating Conditions

| No. | Parameter                         | Symbol     | Condition                                   | Range                   | Unit               | Applied Pin     |
|-----|-----------------------------------|------------|---|-------------------------|--------------------|-----------------|
| 1   | Power supply voltage              | $AV_{DD}$  | $AV_{DD} = DV_{DD}$                         | 2.7 to 3.3              | V                  | $AV_{DD}$       |
|     |                                   | $DV_{DD}$  |   |                         |                    | $DV_{DD}$       |
| 2   | Crystal oscillation frequency     | $f_{XTAL}$ | —   | 8.192 MHz $\pm$ 100 ppm | —                  | XTAL1,<br>XTAL2 |
| 3   | FM multiplex signal input voltage | $V_{AIN}$  | Composite signal including multiplex signal | 0.2 to 0.9*             | $V_{P-P}$          | AIN             |
| 4   | Operating temperature             | $T_a$      | —   | -20 to +75              | $^{\circ}\text{C}$ | —               |

\* The gain of the variable gain amplifier (VGain):  $\times 1$ ,  $\times 1.5$ ,  $\times 2$ , or  $\times 3$ .

The VGain should be adjusted to satisfy the equation:  $V_{AIN} \times \text{VGain} = 0.6 \text{ V to } 0.9 \text{ V}$ .

### 4.2.3 DC Characteristics

( $DV_{DD} = AV_{DD} = 3\text{ V} \pm 10\%$ ,  $DGND = AGND = 0\text{ V}$ ,  $T_a = -20\text{ to }+75^\circ\text{C}$ )

| No. | Parameter                  | Symbol     | Condition   | Min.                 | Typ. | Max.                 | Unit          | Applied Pin   |
|-----|----------------------------|------------|---|----------------------|------|----------------------|---------------|---|
| 1   | Input voltage              | $V_{IH}$   | —   | $0.8 \times DV_{DD}$ | —    | —                    | V             | $\overline{WR}$ , $\overline{RD}$ ,<br>$\overline{XOUTC}$ ,<br>DB0 to DB7,<br>XTAL1, $\overline{CS}$ ,<br>A0 to A5, $\overline{CLR}$ ,<br>$\overline{IORD}$ , $\overline{IOWR}$ |
|     |                            | $V_{IL}$   |   | —                    | —    | $0.2 \times DV_{DD}$ |               |   |
| 2   | Output voltage             | $V_{OH}$   | $I_{OH} = -1\text{ mA}$                             | $DV_{DD}$<br>-0.5    | —    | —                    | V             | MOUT0 to<br>MOUT6, $\overline{INT}$ ,<br>DB0 to DB7,<br>XOUT  |
|     |                            | $V_{OL}$   | $I_{OL} = 2\text{ mA}$                              | —                    | —    | 0.45                 |               |   |
| 3   | Input current 1            | $I_{IH1}$  | $V_{IH} = DV_{DD}$                                  | —                    | —    | 2                    | $\mu\text{A}$ | $\overline{WR}$ , $\overline{RD}$ , $\overline{CS}$ ,<br>DB0 to DB7,<br>A0 to A5,<br>$\overline{CLR}$   |
|     |                            | $I_{IL1}$  | $V_{IL} = DGND$                                     | -2                   | —    | —                    |               |   |
| 4   | Input current 2            | $I_{IH2}$  | $V_{IH} = AV_{DD}$                                  | —                    | —    | 2                    | $\mu\text{A}$ | ADETIN  |
|     |                            | $I_{IL2}$  | $V_{IL} = AGND$                                     | -2                   | —    | —                    |               |   |
| 5   | Input current 3            | $I_{IH3}$  | $V_{IH} = DV_{DD}$                                  | —                    | —    | 2                    | $\mu\text{A}$ | $\overline{XOUTC}$ ,<br>$\overline{IORD}$ , $\overline{IOWR}$   |
| 6   | Pull-up current            | $I_{pull}$ | $DV_{DD} = 3\text{ V}$ ,<br>$V_{IL} = DGND$         | 3                    | 13   | 50                   | $\mu\text{A}$ |   |
| 7   | Output off-leakage current | $I_{OH}$   | $V_{OH} = AV_{DD}$<br>During nonmonitoring (Hiz)    | —                    | —    | 2                    | $\mu\text{A}$ | MON   |
|     |                            | $I_{OL}$   | $V_{OL} = AGND$<br>During nonmonitoring (Hiz)       | -2                   | —    | —                    |               |   |
| 8   | Supply current             | $I_{DD}$   | During operation, no load<br>$f = 8.192\text{ MHz}$ | —                    | 13   | 22                   | mA            | $AV_{DD}$ , $DV_{DD}$   |
|     |                            |            | During power down,<br>no load                       | —                    | —    | 10                   | $\mu\text{A}$ |   |

#### 4.2.4 AC Characteristics

| No. | Parameter  | Symbol*       | Condition  | Min. | Typ. | Max. | Unit    | Applied Pin  |
|-----|--|---------------|--|------|------|------|---------|--|
| 1   | Write setup time                                       | $t_{SWR1}$    | —  | 10   | —    | —    | ns      | $\overline{WR}$ , $\overline{CS}$ ,<br>A0 to A5,<br>DB0 to DB7 |
|     |  | $t_{SWR2}$    | —  | 120  | —    | —    |         |  |
| 2   | Write hold time  | $t_{HWR}$     | —  | 10   | —    | —    | ns      | $\overline{WR}$ , $\overline{CS}$ ,<br>A0 to A5,<br>DB0 to DB7 |
| 3   | Write pulse width                                      | $t_{WWR}$     | —  | 130  | —    | —    | ns      | $\overline{WR}$  |
| 4   | Read setup time  | $t_{SRD}$     | —  | 10   | —    | —    | ns      | $\overline{RD}$ , $\overline{CS}$ ,<br>A0 to A5                |
| 5   | Read hold time   | $t_{HRD}$     | —  | 10   | —    | —    | ns      | $\overline{RD}$ , $\overline{CS}$ ,<br>A0 to A5                |
| 6   | Read pulse width                                       | $t_{WRD}$     | —  | 160  | —    | —    | ns      | $\overline{RD}$  |
| 7   | Interval between error correction data write and write | $t_{IWRWRE}$  | Error correction                                 | 250  | —    | —    | ns      | $\overline{WR}$  |
| 8   | Interval between error correction data read and read   | $t_{IRDRDE}$  | Error correction                                 | 250  | —    | —    | ns      | $\overline{RD}$  |
| 9   | Interval between error correction data write and read  | $t_{IWRRDE}$  | Error correction                                 | 100  | —    | —    | ns      | $\overline{WR}$ ,<br>$\overline{RD}$                           |
| 10  | Interval between layer 4 data clear and write          | $t_{ICLRWR4}$ | Layer 4 CRC                                      | 100  | —    | —    | ns      | $\overline{WR}$  |
| 11  | Interval between layer 4 data write and write          | $t_{IWRWR4}$  | Layer 4 CRC                                      | 4.5  | —    | —    | $\mu s$ | $\overline{WR}$  |
| 12  | Interval between layer 4 data write and read           | $t_{IWRRD4}$  | Layer 4 CRC                                      | 4.5  | —    | —    | $\mu s$ | $\overline{WR}$ ,<br>$\overline{RD}$                           |
| 13  | Read data output delay (1)                             | $t_{DRD1}$    | —  | —    | —    | 160  | ns      | $\overline{RD}$ ,<br>DB0 to DB7                                |
| 14  | Read data output delay (2)                             | $t_{DRD2}$    | —  | —    | —    | 160  | ns      | $\overline{RD}$ ,<br>DB0 to DB7                                |
| 15  | Interrupt CLR delay                                    | $t_{DINTCLR}$ | Step out interrupt<br>Error correction interrupt | 250  | —    | —    | ns      | $\overline{INT}$ ,<br>$\overline{WR}$                          |
| 16  | Error correction time (Horizontal direction)           | $t_{ERRL}$    | —  | —    | —    | 274  | $\mu s$ | $\overline{INT}$ ,<br>DB0                                      |
| 17  | Error correction time (Vertical direction)             | $t_{ERRV}$    | —  | —    | —    | 2178 | $\mu s$ | $\overline{INT}$ ,<br>DB0                                      |
| 18  | CLR pulse width  | $t_{WCLR}$    | —  | 200  | —    | —    | ns      | $\overline{CLR}$   |

\* See section 4.3, "TIMING DIAGRAM".

#### 4.2.5 Filter Characteristics

| No. | Parameter                      | Symbol | Condition   | Min. | Typ. | Max. | Unit | Applied Pin |
|-----|--------------------------------|--------|---|------|------|------|------|-------------|
| 1   | BPF pass band attenuation      | GAIN1  | 72 to 80 kHz<br>Variable gain amplifier<br>gain: 0 dB   | —    | —    | 3.0  | dB   | MON         |
| 2   | BPF block band attenuation (1) | GAIN2  | 0 to 53 kHz<br>Variable gain amplifier<br>gain: 0 dB    | 50   | —    | —    | dB   | MON         |
| 3   | BPF block band attenuation (2) | GAIN3  | 100 to 500 kHz<br>Variable gain amplifier<br>gain: 0 dB | 50   | —    | —    | dB   | MON         |

### 4.3 TIMING DIAGRAM

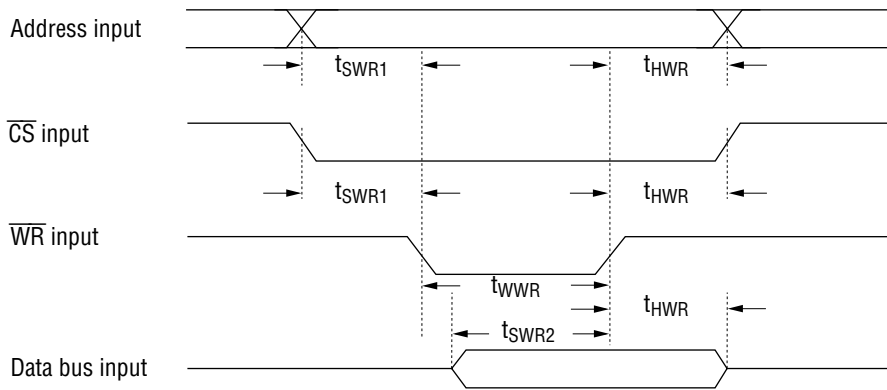


Figure 4.1 Write Timing

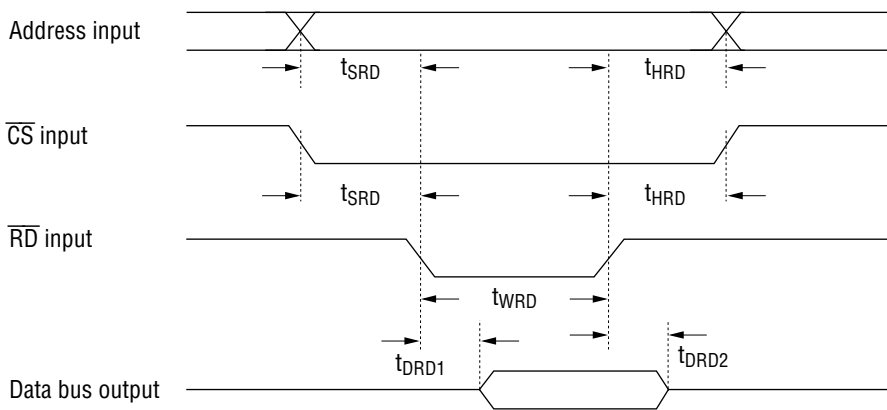
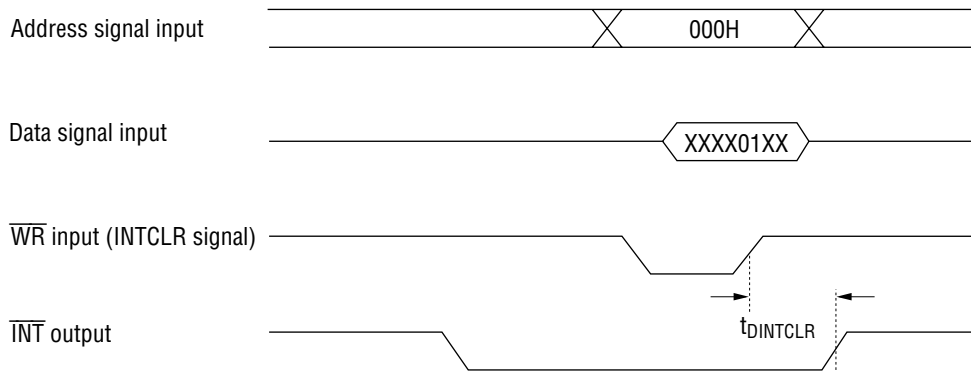


Figure 4.2 Read Timing





**Figure 4.3 Interrupt CLR Timing**

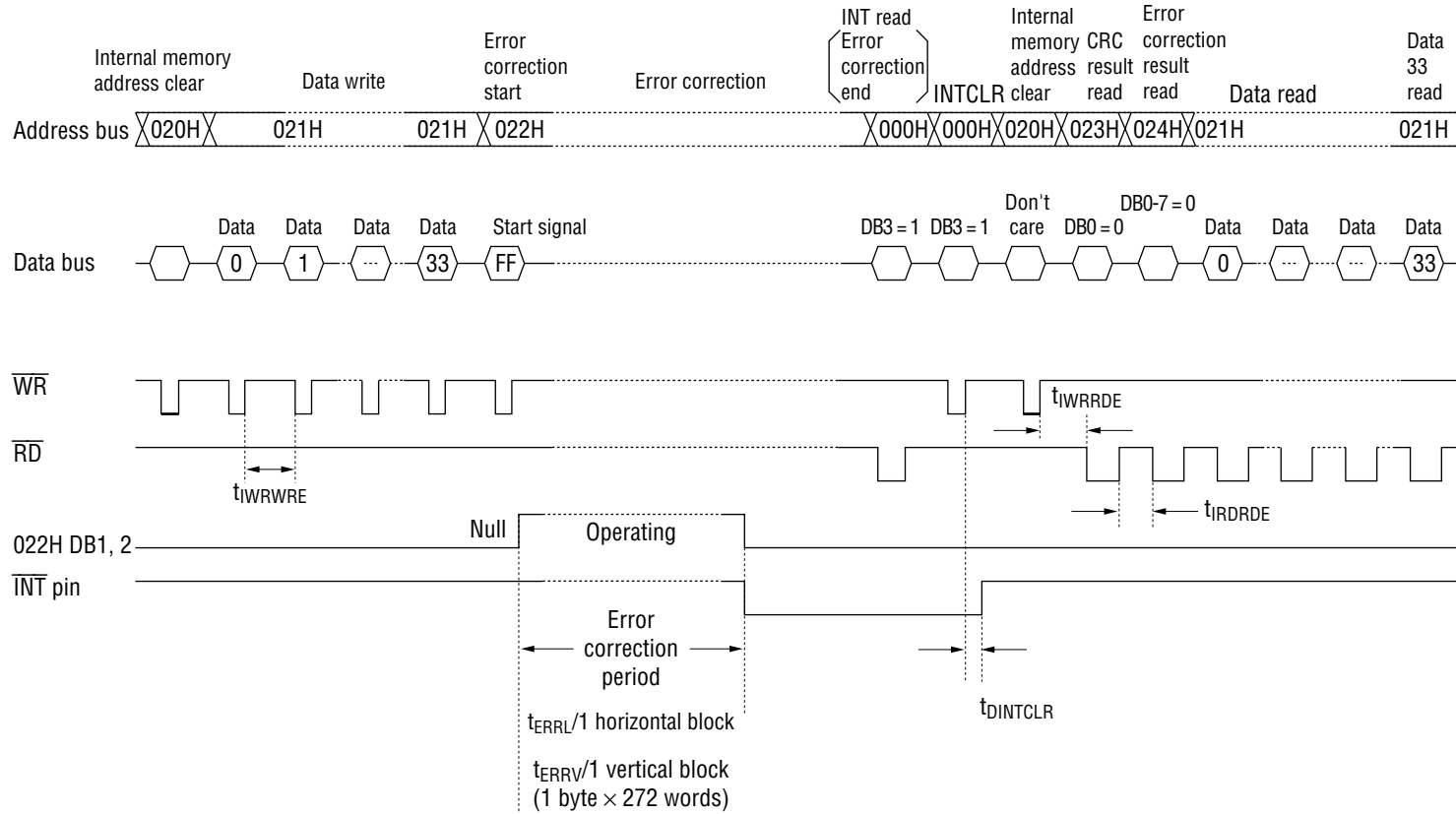
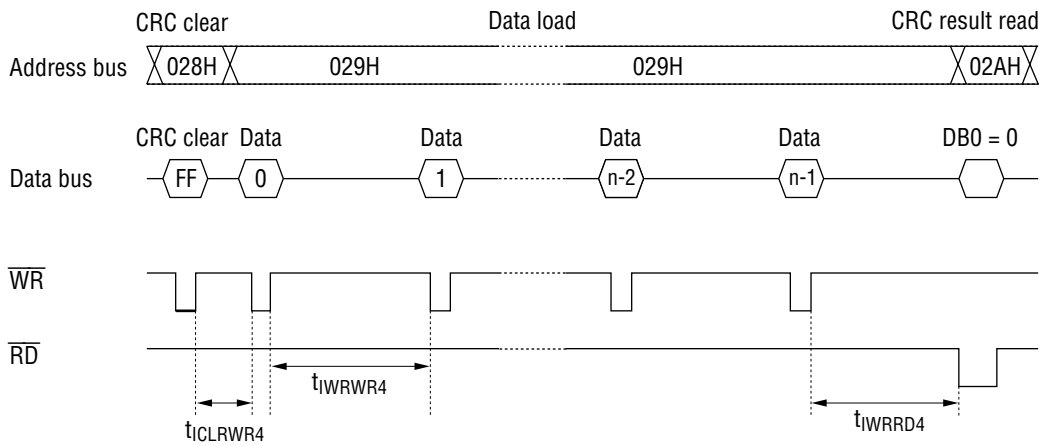


Figure 4.4 Error Correction Timing Diagram



**Figure 4.5 Layer 4 CRC Timing Diagram**

## *Chapter 5*

# **CONTROL REGISTERS**

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## 5. CONTROL REGISTERS

### 5.1 INTERRUPT REGISTERS

#### 5.1.1 Interrupt source

These registers indicate the four types of interrupt factors: (1) receive interrupt, (2) 1st horizontal error correction completion, (3) out of sync., and (4) vertical error correction/2nd horizontal error correction completion. When an interrupt occurs, "1" is written. The registers must be externally cleared after reading, however clear conditions are different for each interrupt factor. For details see Table 5.1.1.

| Address |                      | DB7 | DB6 | DB5 | DB4 | (4)            | (3)            | (2)            | (1)            |
|---------|----------------------|-----|-----|-----|-----|----------------|----------------|----------------|----------------|
|         |                      |     |     |     |     | DB3            | DB2            | DB1            | DB0            |
| 000H    | Reset value          | —   | —   | —   | —   | 0              | 0              | 0              | 0              |
|         | Read/write<br>(Note) | —   | —   | —   | —   | Read/<br>write | Read/<br>write | Read/<br>write | Read/<br>write |

(Note) Write is used to clear the interrupt.  
Write = "1" : clear  
Write = "0" : none

**Table 5.1.1 Interrupt Sources**

| Type   | Generation Condition  | Generation Cycle  | Clear Condition   |
|--|---|---|---|
| INT0<br>Receive interrupt<br>(000H, DB0)                                   | At the time one block is received in a frame/block synchronization state.<br>(Data is received only in a synchronized status; not received in an out-of-sync. state.) | Every time 34 bytes are received (18 ms).   | 1. Write DB0 = "1" to INT (000H).<br>2. Clear the $\overline{\text{CLR}}$ pin.<br>(Initial setting) |
| INT1<br>1st horizontal error correction completion<br>(000H, DB1)          | At the time 1st horizontal error correction is completed.   | 0.274 ms after 1st error correction start signal is written.  | 1. Write DB1 = "1" to INT (000H).<br>2. Clear the $\overline{\text{CLR}}$ pin.<br>(Initial setting) |
| INT2<br>Out of synchronization<br>(000H, DB2)                              | When frame is out of synchronization.   | $\left( \frac{272}{4} \times \left( \frac{\text{number of forward}}{\text{protection steps}} + 123 \right) - 13 \right) \times 18 \text{ ms}$<br><br>This comes out at 10 to 12 seconds when the number of forward protection steps is 8. | 1. Write DB2 = "1" to INT (000H).<br>2. Clear the $\overline{\text{CLR}}$ pin.<br>(Initial setting) |
| INT3<br>Vertical/horizontal 2nd error correction completion<br>(000H, DB3) | At the time error correction is completed.  | When the time shown in the table below has elapsed after an error correction start signal is written (see table below).   | 1. Write DB3 = "1" to INT (000H).<br>2. Clear the $\overline{\text{CLR}}$ pin.<br>(Initial setting) |

|            | Error | Time     | Data      |
|------------|-------|----------|-----------|
| Horizontal | No*   | 0.138 ms | 34 bytes  |
|            | Yes   | 0.274 ms |           |
| Vertical   | No*   | 1.090 ms | 272 bytes |
|            | Yes   | 2.178 ms |           |

\*Error correction is skipped when there is no error.

### 5.1.2 INT Mask

This register controls interrupt generation.

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | (1) |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | —   | —   | —   | —   | DB3 | DB2 | DB1 | DB0 |
| 001H    | Write      |             | —   | —   | —   | —   | 0   | 0   | 0   | 0   |

- (1) DB0-DB3:  
 0: INT0-INT3 interrupt disabled  
 1: INT0-INT3 interrupt enabled  
 INT0: Receive interrupt  
 INT1: 1st horizontal error correction completion interrupt  
 INT2: Out-of-sync interrupt  
 INT3: Vertical/2nd horizontal error correction completion interrupt

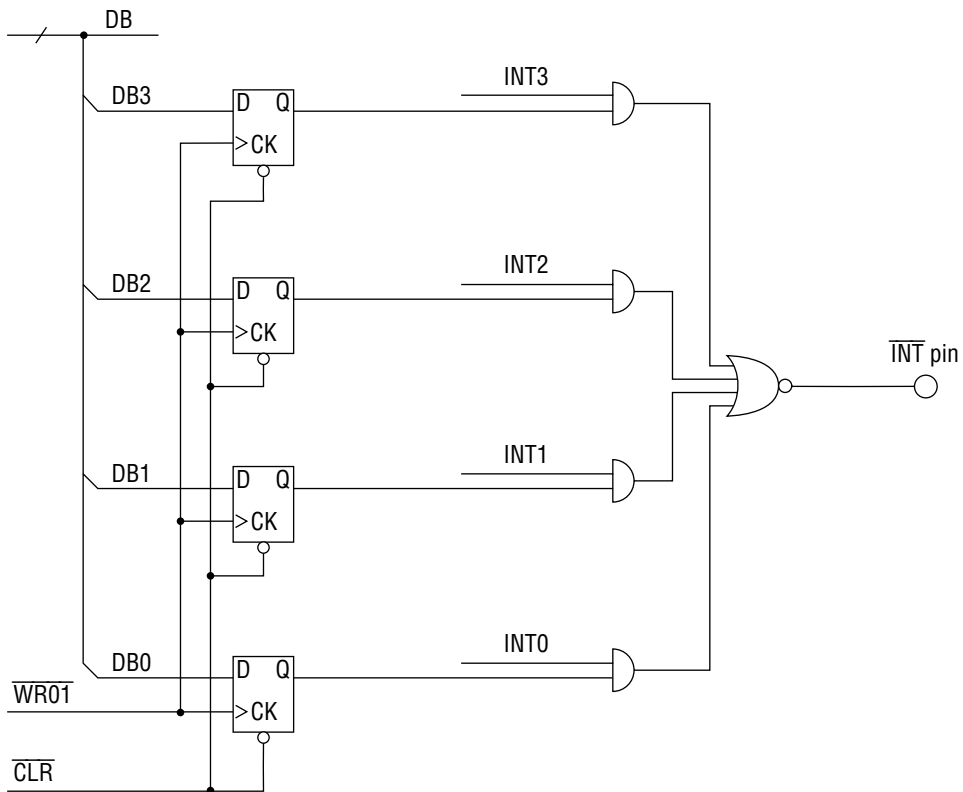


Figure 5.1.1 INT Mask Register

## 5.2 RECEIVE DATA REGISTERS

### 5.2.1 Receive Block Status

This register indicates the status of the received block data, which consists of the following:

(1) Frame Number Change, (2) Frame Number, (3) Block Synchronization Status, (4) Parity Block Indication, (5) Frame Synchronization Status, (6) Layer 2 CRC Result, and (7) Real Time Block Indication

| Address | Read/write | Reset value | (7) | (6) | (5) | (4) | (3) | (2) | (1) |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 |
| 002H    | Read       |             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

(1) DB0: FNCHG (Frame Number Change)

0: No frame number changed

1: "1" is indicated when receive data is the first data (2nd byte) of block number 1, 14, 137, 150 for Method A, and block numbers 1, 61, 131, 191 for Method B.

(2) DB1-DB2: Frame Number

Indicates that the receive data is data of the following block number groups.

|     |     | Receive Data                             |  |
|-----|-----|--|--|
| DB2 | DB1 | Method B                                 | Method A   |
| 0   | 0   | Receive data of block numbers 1 to 13    | Receive data of block numbers 1 to 60  |
| 0   | 1   | Receive data of block numbers 14 to 136  | Receive data of block numbers 61 to 130  |
| 1   | 0   | Receive data of block numbers 137 to 149 | Receive data of block numbers 131 to 190   |
| 1   | 1   | Receive data of block numbers 150 to 272 | Receive data of block numbers 191 to 272 (Method A0)<br>Receive data of block numbers 191 to 284 (Method A1) |

(3) DB3: Block Synchronization Status

0: Indicates receive data in a block out-of-sync state

1: Indicates receive data in a block sync state

(4) DB4: Parity Block Indication

This bit indication is available only in a frame synchronization state.

0: Receive data is not the data of the parity block.

1: Receive data is of the parity block.



(5) DB5: Frame Synchronization Status Indication

- 0: Receive data is in a frame out of sync state.
- 1: Receive data is in a frame sync state.

(6) DB6: CRC Result Indication

- 0: Indicates that the CRC result for the receive data is normal.
- 1: Indicates that the CRC result for the receive data is an error.

(7) DB7: REAL Block Indication

This indication is used for receive block data in a frame sync state when frame A is set in the frame method register (01FH).

- 0: Receive data is not of the REAL block.
- 1: Receive data is of the REAL block.

### 5.2.2 Receive Data RAM Port

This port is used for one block receive data RAM of 34 bytes excluding BIC.

When an interrupt occurs, the internal memory addresses are cleared to zero.

Since the next receive data is output at the rising edge of an RD03 signal, 34 bytes can be read successively.

The status of receive data is shown in 5.2.1.

| Address | Read/write | Reset value | (1)       |           |           |           |           |           |           |           |
|---------|------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|         |            |             | DB7       | DB6       | DB5       | DB4       | DB3       | DB2       | DB1       | DB0       |
| 003H    | Read       |             | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
|         |            |             | b7        | b6        | b5        | b4        | b3        | b2        | b1        | b0        |

### 5.2.3 Receive RAM, Data Accumulation Condition, and Address Clear

(1) DB1: This register specifies the condition (frame/block synchronization) for accumulating data into the receive RAM.

If any data is written to this register, the receive RAM addresses are cleared to zero.

Write the following data before reading the receive RAM second time and thereafter.

0: Receive data is accumulated in receive RAM when the frame is synchronized.

1: Receive data is accumulated in receive RAM when the block is synchronized.

However, when frame synchronization is entered, receive data is accumulated even if the block is out of sync.

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 004H    | Write      |             | —   | —   | —   | —   | —   | —   | 0   | —   |

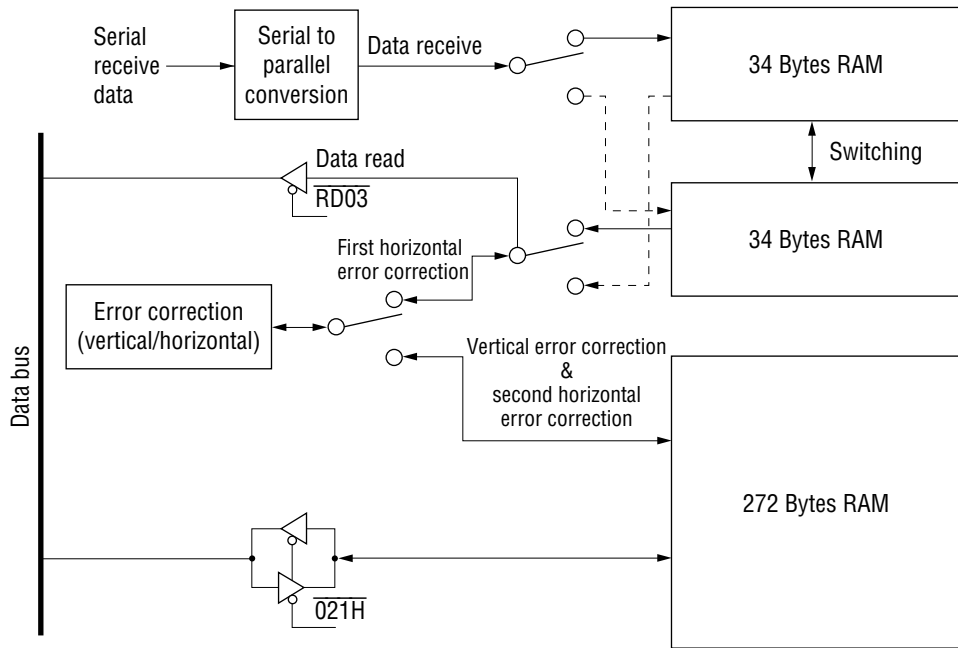
### 5.2.4 BIC Monitor

This register indicates the block identification code (BIC) of the block receive data.

| Address | Read/Write | Reset<br>value | DB7 | DB6 | DB5 | DB4 | DB3 | (1) |     | (2) |
|---------|------------|----------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |                |     |     |     |     |     | DB2 | DB1 | DB0 |
| 007H    | Read       |                | —   | —   | —   | —   | —   | 0   | 0   | 0   |

- (1) DB2: When BIC is detected, "1" is indicated.
- (2) DB0 - DB1: The detected BIC is output as shown below.

| DB1 | DB0 | BIC number |
|-----|-----|------------|
| 0   | 0   | BIC 1      |
| 0   | 1   | BIC 2      |
| 1   | 0   | BIC 3      |
| 1   | 1   | BIC 4      |



**Figure 5.2.1 Receive RAM Configuration**

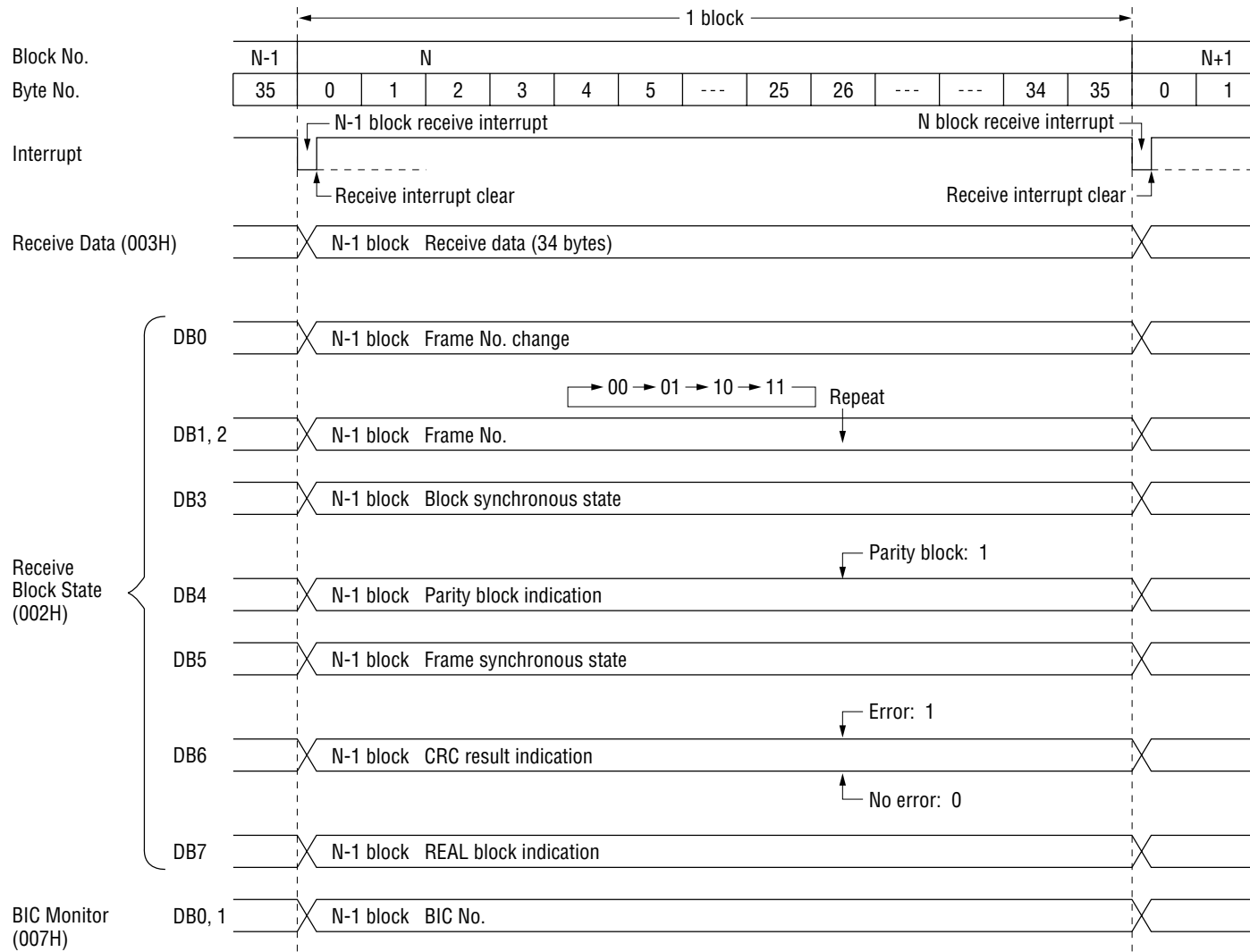


Figure 5.2.2 Receive Data Timing Diagram

## 5.3 CLOCK REGENERATION REGISTERS

### 5.3.1 Fixed Phase Adjustment

This register adjusts the phase of a 16 kHz data sampling clock in 1/125 steps within the range of  $-1/5$  to  $+24/125$ . This register is used for initial settings.

| Address | Read/write | Reset value | (3) | (2) |     |     | (1) |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 008H    | Write      |             | —   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

(1) DB0-DB2: Phase delay settings in 1/125 steps

| DB2 | DB1 | DB0 | Phase Delay Setup Value |
|-----|-----|-----|-------------------------|
| 0   | 0   | 0   | 0/125                   |
| 0   | 0   | 1   | 1/125                   |
| 0   | 1   | 0   | 2/125                   |
| 0   | 1   | 1   | 3/125                   |
| 1   | 0   | 0   | 4/125                   |
| 1   | 0   | 1   | Inhibit                 |
| 1   | 1   | 0   | Inhibit                 |
| 1   | 1   | 1   | Inhibit                 |

(2) DB3-DB5: Phase delay settings in 1/25 steps

| DB5 | DB4 | DB3 | Phase Delay Setup Value |
|-----|-----|-----|-------------------------|
| 0   | 0   | 0   | 0/25                    |
| 0   | 0   | 1   | 1/25                    |
| 0   | 1   | 0   | 2/25                    |
| 0   | 1   | 1   | 3/25                    |
| 1   | 0   | 0   | 4/25                    |
| 1   | 0   | 1   | Inhibit                 |
| 1   | 1   | 0   | Inhibit                 |
| 1   | 1   | 1   | Inhibit                 |

(3) DB6: Phase advance setting in 1/5 steps

| DB6 | Phase Lead Setup Value |
|-----|------------------------|
| 0   | 0                      |
| 1   | 1/5                    |

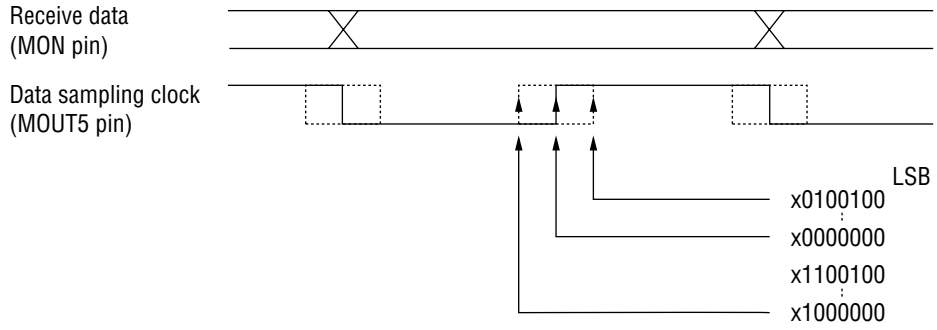


Figure 5.3.1 Phase Adjustment

### 5.3.2 Bit Gate

This register sets the gate width centered around the rising edge of the data clock. Gate width can be changed depending on parameters set before and after block synchronization.

This function is for varying the constant of integration for the clock sampling timing detected inside and outside the gate. This register is used for initial settings.

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | (2) |     | (1) |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | —   | —   | —   | —   | DB3 | DB2 | DB1 | DB0 |
| 009H    | Write      |             | —   | —   | —   | —   | 0   | 0   | 0   | 0   |

(1) DB0-DB1: Before block synchronization

(2) DB2-DB3: After block synchronization

| After Block Synchronization |     | Before Block Synchronization |     | Gate   |      |
|-----------------------------|-----|------------------------------|-----|--------|------|
| DB3                         | DB2 | DB1                          | DB0 |        |      |
| 0                           | 0   | 0                            | 0   | Gate 0 |      |
| 0                           | 1   | 0                            | 1   | Gate 1 | ±10% |
| 1                           | 0   | 1                            | 0   | Gate 2 | ±20% |
| 1                           | 1   | 1                            | 1   | Gate 3 | ±30% |

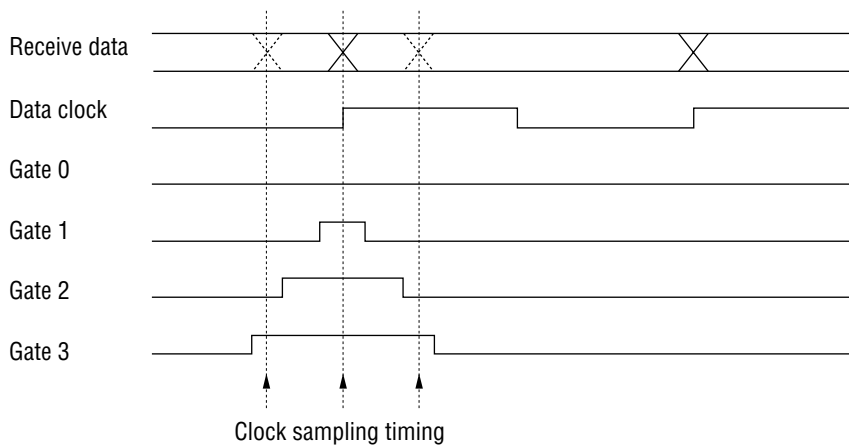


Figure 5.3.2 Clock Sampling Gate



### 5.3.3 Integration Constant

This register sets the timing sampling count required for phase control. The parameters are before and after block synchronization, and inside and outside the gate. This register is used for initial settings.

(1) Integration constant before block synchronization, outside the gate (0-15)

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 00AH    | Write      |             | —   | —   | —   | —   | 0   | 0   | 1   | 0   |

(2) Integration constant before block synchronization, inside the gate (0-15)

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 00BH    | Write      |             | —   | —   | —   | —   | 0   | 0   | 1   | 0   |

(3) Integration constant after block synchronization, outside the gate (0-63)

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 00CH    | Write      |             | —   | —   | 0   | 1   | 1   | 0   | 0   | 0   |

(4) Integration constant after block synchronization, inside the gate (0-63)

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 00DH    | Write      |             | —   | —   | 0   | 1   | 1   | 0   | 0   | 0   |

### 5.3.4 Phase Correction Step

This register sets the phase correction step width of DPLL used for data clock regeneration. This register can be used to adjust data clock supply speeds or data clock jitter control. Phase correction step widths can be changed depending on parameters set before or after block synchronization. This register is used for initial settings.

| Address | Read/write | Reset value |     |     |     |     | (2) |     | (1) |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 00EH    | Write      |             | —   | —   | —   | —   | 0   | 1   | 0   | 1   |
|         |            |             |     |     |     |     | b1  | b0  | b1  | b0  |

Time constants can be set as shown in Table 5.3.1 by combining the integration constants shown in Sections 5.3.3 and 5.3.4.

**Table 5.3.1 Phase Correction Step**

| Integration Constant |        |                       | After Block Synchronization                          |             |             |     |             |     |             |     |             |     |             |     |             |
|----------------------|--------|-----------------------|--|-------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|
|                      |        |                       | Before Block Synchronization                         |             |             |     |             |     |             |     |             |     |             |     |             |
|                      |        |                       | 1  | 2           | ---         | 4   | ---         | 8   | ---         | 16  | ---         | 32  | ---         | 64  |             |
| b<br>1               | b<br>0 | Phase Correction Step | 1/4 MHz<br>(= 0.4% = 4000 ppm)                       | 4000 ppm    | 2000 ppm    | --- | 1000 ppm    | --- | 500 ppm     | --- | 250 ppm     | --- | 125 ppm     | --- | 62.5 ppm    |
|                      |        |                       | Packet count required for a 1-bit phase displacement | 0.69 Packet | 1.38 Packet | --- | 2.77 Packet | --- | 5.55 Packet | --- | 11.1 Packet | --- | 22.2 Packet | --- | 44.4 Packet |
| 0                    | 0      | Phase Correction Step | 2/4 MHz<br>(= 0.8% = 8000 ppm)                       | 8000 ppm    | 4000 ppm    | --- | 2000 ppm    | --- | 1000 ppm    | --- | 500 ppm     | --- | 250 ppm     | --- | 125 ppm     |
|                      |        |                       | Packet count required for a 1-bit phase displacement | 0.34 Packet | 0.69 Packet | --- | 1.38 Packet | --- | 2.77 Packet | --- | 5.55 Packet | --- | 11.1 Packet | --- | 22.2 Packet |
| 1                    | 0      | Phase Correction Step | 4/4 MHz<br>(= 1.6% = 16000 ppm)                      | 16000 ppm   | 8000 ppm    | --- | 4000 ppm    | --- | 2000 ppm    | --- | 1000 ppm    | --- | 500 ppm     | --- | 250 ppm     |
|                      |        |                       | Packet count required for a 1-bit phase displacement | 0.17 Packet | 0.34 Packet | --- | 0.69 Packet | --- | 1.38 Packet | --- | 2.77 Packet | --- | 5.55 Packet | --- | 11.1 Packet |
| 1                    | 1      | Phase Correction Step |  | 0.17 Packet | 0.34 Packet | --- | 0.69 Packet | --- | 1.38 Packet | --- | 2.77 Packet | --- | 5.55 Packet | --- | 11.1 Packet |

## 5.4 BLOCK SYNCHRONIZATION REGISTERS

### 5.4.1 Allowable Number of BIC Error Bits

This register specifies how many erroneous bits can be allowed in the block identification code (BIC). Values can be changed depending on parameter values before and after block synchronization. This register is used for initial settings.

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | (2) |     | (1) |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             |     |     |     |     | DB3 | DB2 | DB1 | DB0 |
| 010H    | Write      |             | —   | —   | —   | —   | 0   | 1   | 1   | 0   |

(1) Allowable number of erroneous BIC bits before block synchronization

| DB1 | DB0 | Allowable Number of Erroneous Bits in BIC Before Block Synchronization |
|-----|-----|--|
| 0   | 0   | 0  |
| 0   | 1   | 1  |
| 1   | 0   | 2  |
| 1   | 1   | 3  |

(2) Allowable number of erroneous BIC bits after block synchronizaiton

| DB3 | DB2 | Allowable Number of Erroneous Bits in BIC After Block Synchronization |
|-----|-----|---|
| 0   | 0   | 0   |
| 0   | 1   | 1   |
| 1   | 0   | 2   |
| 1   | 1   | 3   |

### 5.4.2 Number of Block Synchronization Backward Protection Steps

This register specifies the number of block synchronization backward protection steps. When block identification codes (BICs) are successively detected for a specified number of times, the internal bit counter and the bit position of the block (0-287) are synchronized. This register is used for initial settings.

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 011H    | Write      |             | —   | —   | —   | —   | —   | —   | 0   | 1   |

(1) DB0-DB1: Number of block synchronization backward protection steps

| DB1 | DB0 | Block proving in synchronization step count |
|-----|-----|---|
| 0   | 0   | Inhibit                                     |
| 0   | 1   | 2   |
| 1   | 0   | 3   |
| 1   | 1   | 4   |

### 5.4.3 Number of Block Synchronization Forward Protection Steps

This register specifies the number of block synchronization forward protection steps. If BICs cannot be detected successively for a specified number of times after block synchronization, the block is regarded as out of synchronization. This register is used for initial settings.

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 012H    | Write      |             | —   | —   | —   | —   | 1   | 0   | 0   | 0   |

(1) DB0-DB3: Number of block synchronization forward protection steps

| DB3 | DB2 | DB1 | DB0 | Number of Block Synchronization Forward Protection Steps |
|-----|-----|-----|-----|--|
| 0   | 0   | 0   | 0   | 0 (Inhibit)  |
| 0   | 0   | 0   | 1   | 1  |
| ⋮   | ⋮   | ⋮   | ⋮   | ⋮  |
| 1   | 1   | 1   | 1   | 15   |

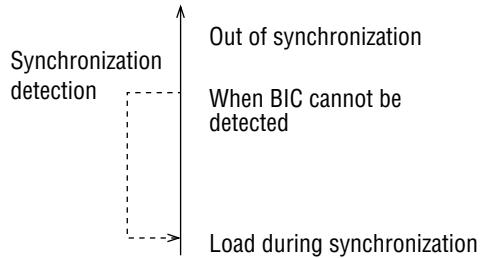
### 5.4.4 Block Synchronization Monitor

- (1) Block synchronization monitoring register (DB0)
- (2) Registers to monitor the number of block synchronization forward protection steps (DB4-DB7). Both (1) and (2) are used for testing.

| Address | Read/write | Reset value | (2) |     |     |     | (1) |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 013H    | Read       |             | 0   | 0   | 0   | 0   | —   | —   | —   | 0   |

- (1) DB0: Monitors block synchronization status.  
 0: block out-of-synchronization  
 1: block synchronized
- (2) DB4-DB7: Monitors the number of block synchronization forward protection steps. While a block is synchronized, if a BIC is not detected in a number of successive attempts, the number of attempts is decremented from the set number of block synchronization forward protection steps; when all the values of DB4 to DB7 change from 1 to 0, it is judged that the block is out of synchronization.

| DB7 | DB6 | DB5 | DB4 | Remaining Number of Block Synchronization Forward Protection Steps |
|-----|-----|-----|-----|--|
| 0   | 0   | 0   | 0   | 0  |
| 0   | 0   | 0   | 1   | 1  |
| ⋮   | ⋮   | ⋮   | ⋮   | ⋮  |
| 1   | 1   | 1   | 1   | 15   |



### 5.4.5 Block Synchronization Set

This register forcibly sets block synchronization, and is used for testing.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 014H    | Write      | value | x   | x   | x   | x   | x   | x   | x   | x   |

x : don't care

### 5.4.6 Block Synchronization Clear

This register forcibly sets block out-of-synchronization. This setting is effective when a channel is changed, in clearing a previous synchronizing status, to permit faster synchronization for the new channel.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 015H    | Write      | value | x   | x   | x   | x   | x   | x   | x   | x   |

x : don't care

### 5.4.7 Bit Number Monitor

These registers monitor bit numbers. They are used for testing.

DB0 of the 017H register is MSB, and DB0 of the 016H register is LSB. Numbers 0 to 287 are displayed.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 016H    | Read       | value | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|         |            |       | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 017H    | Read       | value | —   | —   | —   | —   | —   | —   | —   | 0   |
|         |            |       |     |     |     |     |     |     |     | b8  |

## 5.5 FRAME SYNCHRONIZATION REGISTERS

### 5.5.1 Number of Frame Synchronization Backward Protection Steps

This register specifies the number of times that synchronization points required for frame synchronization have to be detected in succession in order for the frame to be judged as being synchronized. When the block number changing points (= frame synchronization points: 272→1, 13→14, 136→137, and 149→150, under format B) are detected the same number of times as the specified number of successive steps (number of frame synchronization backward protection steps), frame synchronization is entered and the internal frame counter is synchronized with the detected block number.

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 018H    | Write      |             | —   | —   | —   | —   | —   | —   | 0   | 1   |

(1) DB0-DB1: Number of frame synchronization backward protection steps

| DB1 | DB0 | Number of Frame Synchronization Backward Protection Steps |
|-----|-----|---|
| 0   | 0   | 1   |
| 0   | 1   | 2   |
| 1   | 0   | 3   |
| 1   | 1   | 4   |

### 5.5.2 Number of Frame Synchronization Forward Protection Steps

This register specifies the number of times that successive unsuccessful attempts to detect the synchronization points required for frame synchronization that will cause a judgment that a frame is out of synchronization.

After frame synchronization, if the block number changing points (= frame synchronization points: 272→1, 13→14, 136→137, and 149→150, under format B) are not detected the same number of times as the specified number of successive steps (number of frame synchronization forward protection steps), the frame will be out of synchronization to terminate data reception. This register is used for initial settings.

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 019H    | Write      |             | —   | —   | —   | —   | 0   | 1   | 0   | 0   |

(1) DB0-DB3: Number of frame synchronization forward protection steps

| DB3 | DB2 | DB1 | DB0 | Number of Frame Synchronization Forward Protection Steps |
|-----|-----|-----|-----|--|
| 0   | 0   | 0   | 0   | 0 (Inhibit)  |
| 0   | 0   | 0   | 1   | 1  |
| ⋮   | ⋮   | ⋮   | ⋮   | ⋮  |
| 1   | 1   | 1   | 1   | 15   |

### 5.5.3 Frame Synchronization Monitor

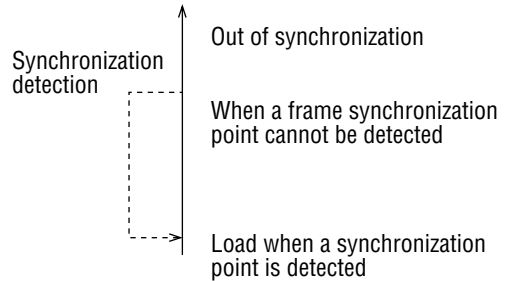
- (1) Frame synchronization monitoring register (DB1)
- (2) Register for monitoring the number of frame synchronization forward protection steps (DB4-DB7)

Both (1) and (2) are for testing.

| Address | Read/write | Reset value | (2) |     |     |     | (1) |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 01AH    | Read       |             | 0   | 0   | 0   | 0   | —   | —   | 0   | —   |

- (1) DB1: Monitors frame synchronization status.  
0: frame out-of-synchronization  
1: frame synchronized
- (2) DB4-DB7: Monitors the number of frame synchronization forward protection steps. While a frame is synchronized, when successive attempts to detect frame synchronization points fail, that number of attempts is decremented from the set number of frame synchronization forward protection steps; when all the values of DB4 to DB7 change from 1 to 0, the frame is judged to be out of synchronization.

| DB7 | DB6 | DB5 | DB4 | Remaining Number of Frame Synchronization Forward Protection Steps |
|-----|-----|-----|-----|--|
| 0   | 0   | 0   | 0   | 0  |
| 0   | 0   | 0   | 1   | 1  |
| ⋮   | ⋮   | ⋮   | ⋮   | ⋮  |
| 1   | 1   | 1   | 1   | 15   |





### 5.5.4 Frame Synchronization Set

This register forcibly sets frame synchronization and is used for testing.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 01BH    | Write      | value | X   | X   | X   | X   | X   | X   | X   | X   |

x : don't care

### 5.5.5 Frame Synchronization Clear

This register forcibly sets frame out-of-synchronization. This function is effective when a channel is changed, in clearing a previous synchronizing status, to permit faster synchronization for the new channel.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 01CH    | Write      | value | X   | X   | X   | X   | X   | X   | X   | X   |

x : don't care

### 5.5.6 Block Number Monitor

These registers monitor block numbers and are used for testing.

DB0 of 01EH register is MSB, and DB0 of 01DH register is LSB. Numbers 0 to 271 are displayed.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 01DH    | Read       | value | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|         |            |       | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 01EH    | Read       | value | —   | —   | —   | —   | —   | —   | —   | 0   |
|         |            |       |     |     |     |     |     |     |     | b8  |



### 5.5.7 Frame Format Specification

| Address | Read/Write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 01FH    | Write      |             | —   | —   | —   | —   | —   | —   | 1   | 0   |

| B1 | B0 | Frame Format | Symbol | Note                                  |
|----|----|--------------|--------|---------------------------------------|
| 0  | 0  | Format A     | A0     | —                                     |
| 0  | 1  |              | A1     | Including realtime information block. |
| 1  | 0  | Format B     | B      | Japan, FMSS                           |
| 1  | 1  | Format C     | C      | —                                     |

## 5.6 ERROR CORRECTION REGISTERS

### 5.6.1 Internal Memory Address Counter Clear

This command clears the address counter of internal memory (set to 0) before writing and reading an error correction data block. Since error correction is executed sequentially from address 0 of internal memory, the internal memory address counter must be cleared before writing.

After error correction, it is necessary to clear the internal memory address counter to read data sequentially from address 0 of internal memory.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 020H    | Write      | value | x   | x   | x   | x   | x   | x   | x   | x   |

x : don't care

### 5.6.2 Data Transfer Port for Error Correction

This port writes data before error correction and reads data after error correction.

When correcting an error in a horizontal (vertical) direction after clearing the internal memory address counter, write 34 (272) bytes of data to this port.

After correcting an error in a horizontal (vertical) direction, clear the internal memory address counter, then read 34 (272) bytes of data from this port.

When reading or writing data for this port, it is unnecessary to specify the horizontal (vertical) direction error correction mode.

| Address | Read/write | Reset | DB7       | DB6       | DB5       | DB4       | DB3       | DB2       | DB1       | DB0       |
|---------|------------|-------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 021H    | Read/write | value | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
|         |            |       | b7        | b6        | b5        | b4        | b3        | b2        | b1        | b0        |

### 5.6.3 Error Correction Start Signal

When start action specification data is written into DB0 to DB2, error correction starts in the specified mode. When error correction is completed, an interrupt is generated.  
The operation status of the error correction circuit can be monitored by this register.

|                |                   |                |            |            |            |            |            |            |            |            |
|----------------|-------------------|----------------|------------|------------|------------|------------|------------|------------|------------|------------|
| <b>Address</b> | <b>Read/write</b> | Reset<br>value | <b>DB7</b> | <b>DB6</b> | <b>DB5</b> | <b>DB4</b> | <b>DB3</b> | <b>DB2</b> | <b>DB1</b> | <b>DB0</b> |
|                |                   |                | —          | —          | —          | —          | —          | 0          | 0          | 0          |

(2) Read  
(1) Write

(1) DB0 - DB2 (Write) : Error correction start mode specification

| <b>DB2</b> | <b>DB1</b> | <b>DB0</b> | <b>Start Action (write)</b>   |
|------------|------------|------------|---|
| 0          | 0          | 1          | Horizontal error correction of receive block data (at address 003H on the 34-byte RAM) starts.<br>Corrected data is written to address 003H on the RAM. |
| 0          | 1          | 0          | Vertical error correction of data written in address 021H on the 272-byte RAM starts.<br>Corrected data is written in address 021H on the RAM.          |
| 1          | 0          | 0          | Horizontal error correction of data written in address 021H on the 34-byte RAM starts.<br>Corrected data is written in address 021H on the RAM.         |

(2) DB0 - DB2 (Read) : Monitor

The data written in this register can be used to monitor the error correction circuit operation status because the data is cleared after error correction is complete.

DB0: Displays the operation status of the horizontal error correction for receive block data.

DB1: Displays the operation status of the vertical error correction.

DB2: Displays the operation status of the 2nd horizontal error correction.

for each of these bits:

0: Error correction circuit is idle.

1: Error correction circuit is in operation.

### 5.6.4 CRC Result Indication

This register indicates a 14-bit CRC result. When horizontal direction error correction is executed, a 14-bit CRC is performed internally on corrected data and the result is indicated. This register is cleared immediately after error correction starts.

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |   |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|---|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |   |
| 023H    | Read       | value       | —   | —   | —   | —   | —   | —   | —   | —   | 0 |

DB0: 14-bit CRC result

0: Normal

1: Error

### 5.6.5 Error Correction Result Indication

This register indicates an error correction result.

If syndrome registers are all 0 after error correction, this register indicates a normal status. If not, it indicates an error. This register is cleared immediately after error correction starts.

In the case of a horizontal-direction correction, the result is indicated at DB7. In the case of a vertical-direction correction, the result is indicated at DB0-DB7 corresponding to bits 0-7.

| Address | Read/write | Reset value | (2) |     |     |     |     |     |     |     |   |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|---|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |   |
| 024H    | Read       | value       | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0 |

(1) DB7: Horizontal-direction error correction result

0: Normal

1: Error

(2) DB0-DB7: Vertical direction error correction result (corresponding to bits 0-7)

0: Normal

1: Error

### 5.6.6 Majority Logic Threshold Value

This register sets the majority logic threshold value for error correction. The setup range is 1 to 17. This register is used for initial settings.

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 025H    | Write      |             | —   | —   | —   | 0   | 1   | 0   | 0   | 0   |

| DB4 | DB3 | DB2 | DB1 | DB0 | Majority Logic Threshold Value |
|-----|-----|-----|-----|-----|--------------------------------|
| 0   | 0   | 0   | 0   | 0   | Inhibit                        |
| 0   | 0   | 0   | 0   | 1   | 1                              |
| ∫   | ∫   | ∫   | ∫   | ∫   | ∫                              |
| 0   | 1   | 0   | 0   | 0   | 8                              |
| ∫   | ∫   | ∫   | ∫   | ∫   | ∫                              |
| 0   | 1   | 1   | 1   | 1   | 15                             |
| 1   | 0   | 0   | 0   | 0   | 16                             |
| 1   | 0   | 0   | 0   | 1   | 17                             |

### 5.6.7 Internal Address Monitor

This register indicates the addresses (0-271) of internal memory for error correction. This is used for testing.

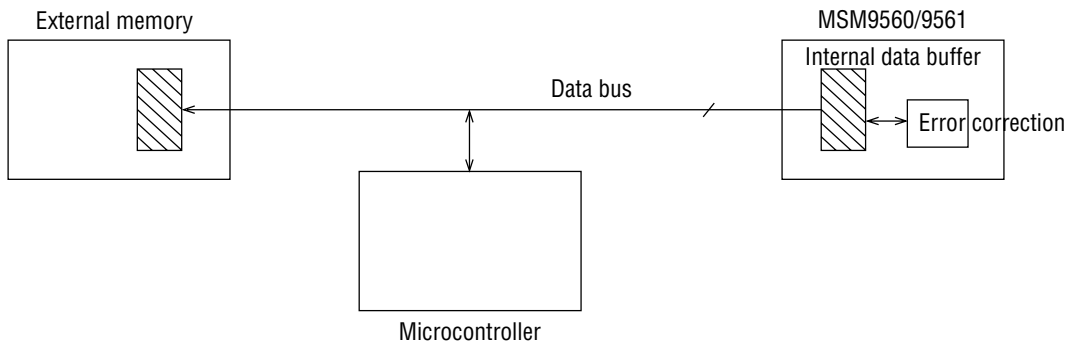
(1)

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 026H    | Read       |             | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|         |            |             | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |

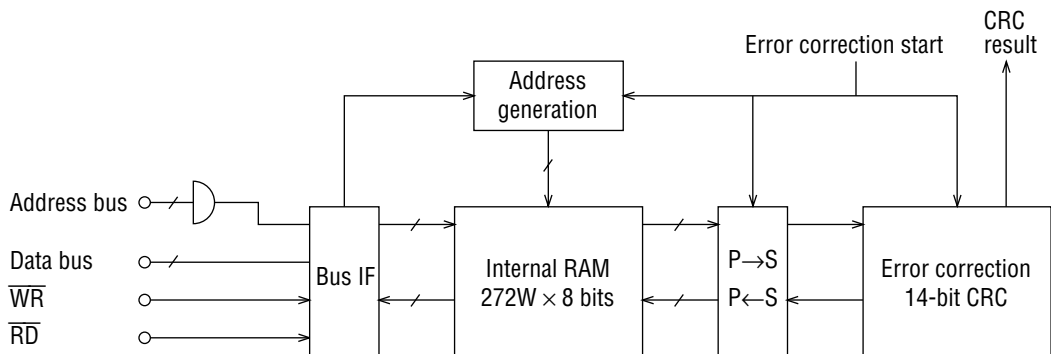
  

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 027H    | Read       |             | —   | —   | —   | —   | —   | —   | —   | 0   |
|         |            |             |     |     |     |     |     |     |     | b8  |

- Error correction involves external RAM, a microcontroller and MSM9552/9553.
- Transfer data in error correction units (horizontal direction equals 34 bytes, vertical direction equals 272 bytes) from external memory to the internal buffer of the MSM9552/9553. Error correction is then executed. Transfer data after error correction from the internal buffer to external memory.



**Figure 5.6.1 General Configuration of Error Correction**

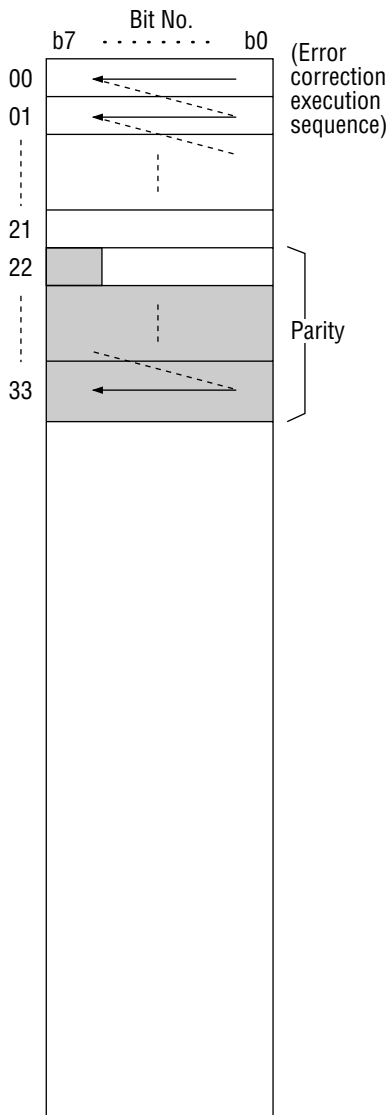


Note: CRC is executed on data after horizontal-direction error correction.

**Figure 5.6.2 Configuration of Error Correction Section**

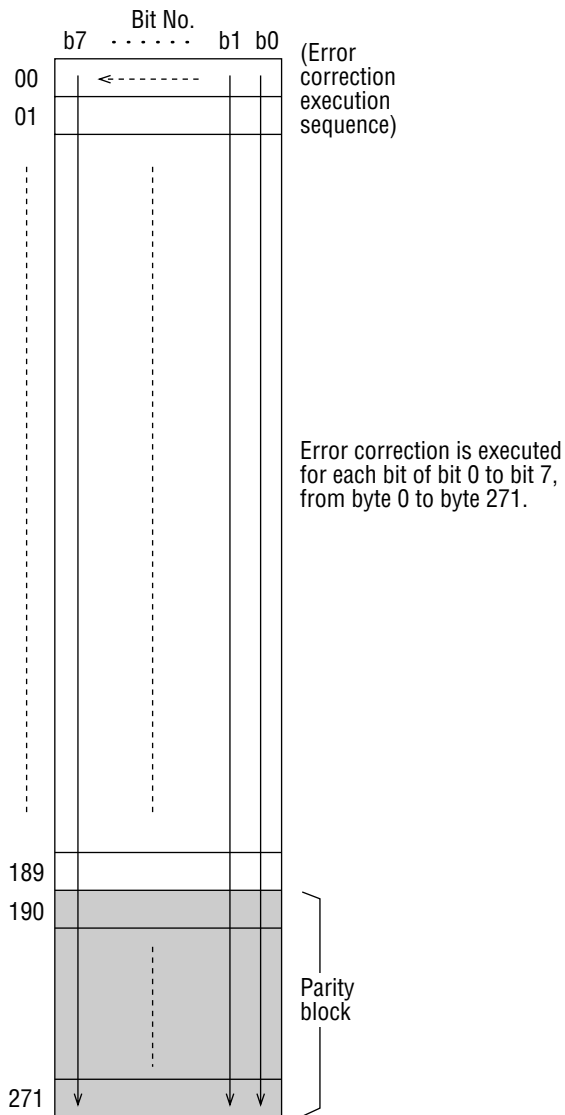


Internal data memory address



Horizontal direction error correction

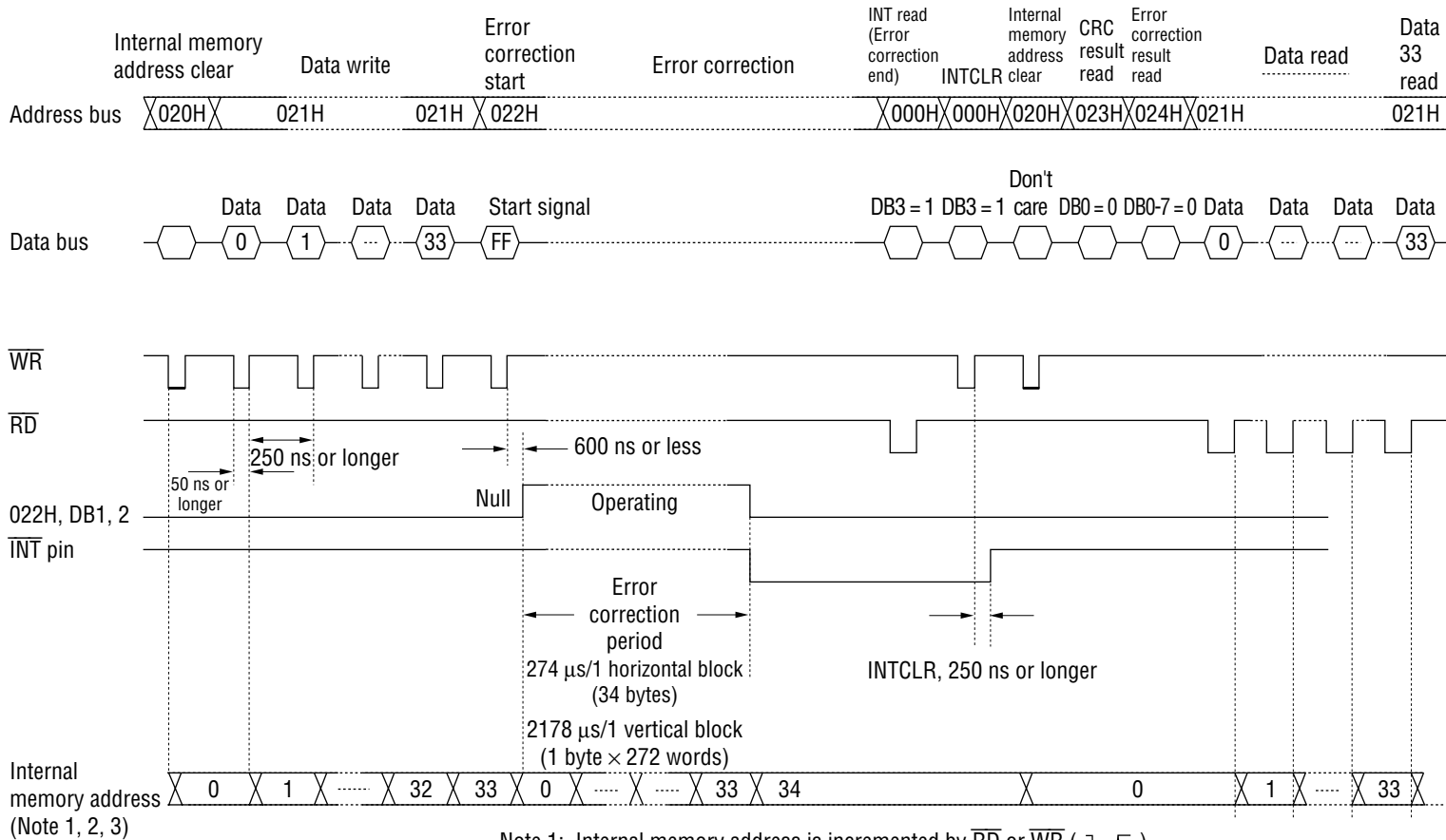
Internal data memory address



Error correction is executed for each bit of bit 0 to bit 7, from byte 0 to byte 271.

←  
Eight times  
Vertical-direction error correction

**Figure 5.6.3 Error Correction Sequence**



Note 1: Internal memory address is incremented by  $\overline{RD}$  or  $\overline{WR}$  (  $\downarrow \uparrow$  ).  
 Note 2: Internal memory address counter is automatically cleared only when error correction starts.  
 Note 3: Internal memory address can be monitored. (The address is the one to be read/written the next time.)

Figure 5.6.4 Error Correction Timing Diagram

## 5.7 LAYER 4 CRC REGISTERS

### 5.7.1 Layer 4 CRC Register Clear

This command clears the CRC register and sets all of its contents to 0 before layer 4 CRC processing. Execute this command once before reading the data group on which CRC processing is to be performed.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 028H    | Write      | value | x   | x   | x   | x   | x   | x   | x   | x   |

x : don't care

### 5.7.2 Layer 4 CRC Data Buffer

Write the data group on which CRC processing is to be performed in byte units with a cycle of 4.5  $\mu$ s or longer. The data written inside the IC is loaded to the CRC operation register and a shift operation is executed (eight times). The system then waits for the next data input.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 029H    | Write      | value | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

### 5.7.3 Layer 4 CRC Result Indication

This register indicates a layer 4 CRC result. After the last data of a data block is written, pause for at least 4.5  $\mu$ s before reading.

| Address | Read/write | Reset | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------|-----|-----|-----|-----|-----|-----|-----|-----|
| 02AH    | Read       | value | —   | —   | —   | —   | —   | —   | —   | 0   |

- (1) DB0: layer 4 CRC result  
 0: Normal  
 1: Error

### 5.7.4 Layer 4 CRC Register

This register is used for writing initial values directly to the CRC operation register, and reading values which are still in progress.

With this function, layer 4 CRC processing for multiple data groups can be performed in parallel. For example, CRC processing for a short data group can be inserted while CRC processing for a long data group is in progress.

#### (1) Layer 4 CRC register high-order 8 bits

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 02BH    | Read/write |             | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|         |            |             | b7  | b6  | b5  | b4  | b3  | b2  | b1  | b0  |

#### (2) Layer 4 CRC register low-order 8 bits

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 02CH    | Read/write |             | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|         |            |             | b15 | b14 | b13 | b12 | b11 | b10 | b9  | b8  |

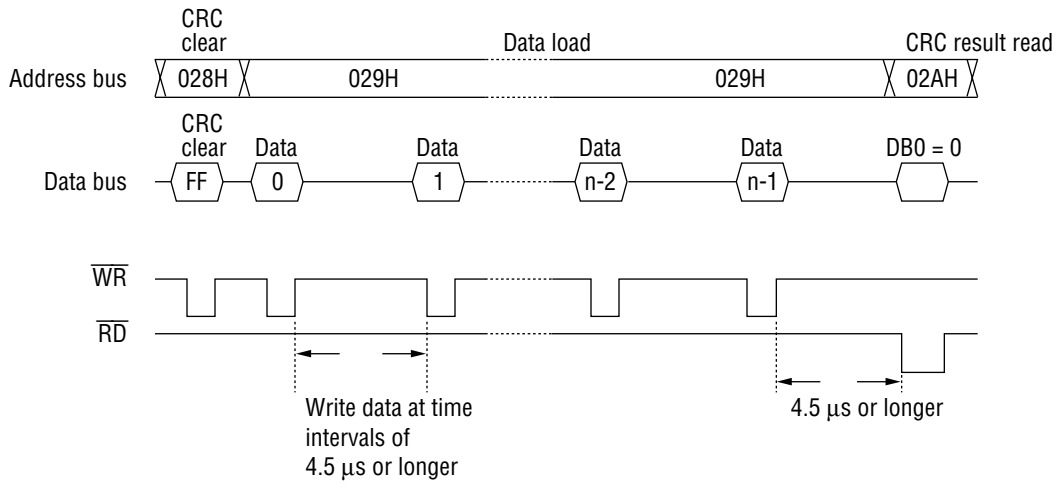
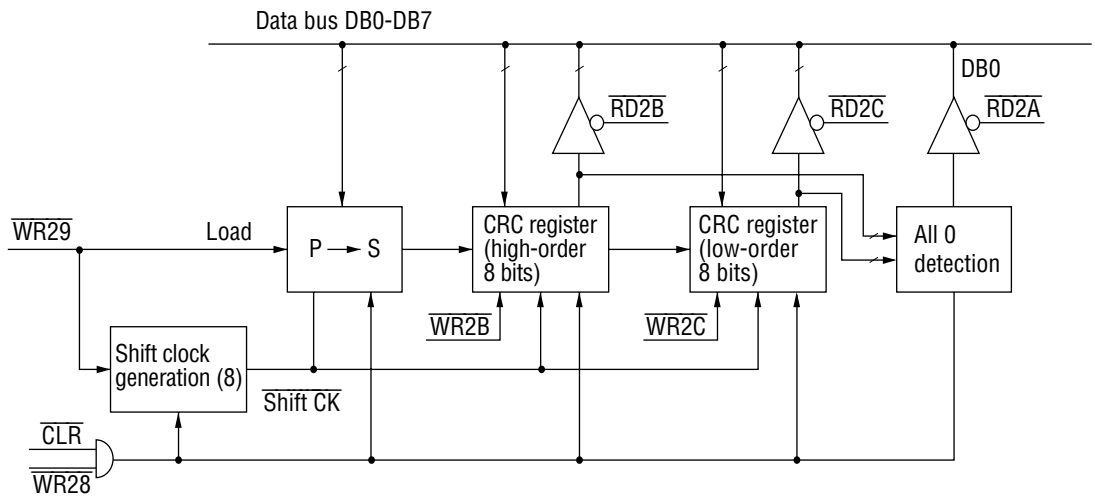


Figure 5.7.1 Layer 4 CRC Block Diagram and Timing Diagram

## 5.8 ANALOG SECTION CONTROL/MONITOR REGISTER

This register is used for level adjustment of the analog input signal (composite signal) and analog section test mode settings.

| Address | Read/write | Reset value | (3) |     |     | (2) |     | (1) |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 |
| 030H    | Write      |             | —   | —   | 0   | 0   | 0   | 0   | 0   |

- (1) DB0: DETC  
Controls the input of analog input pin ADETIN.
- 0: Disables the input of analog input pin ADETIN, so that the input buffer amplifier is powered down (during FM multiplex broadcast reception).
- 1: Enables the input of analog input pin ADETIN, so that the input buffer amplifier is powered on.
- The connections are switched as follows (available for input of a 16 kbps digital test signal) :

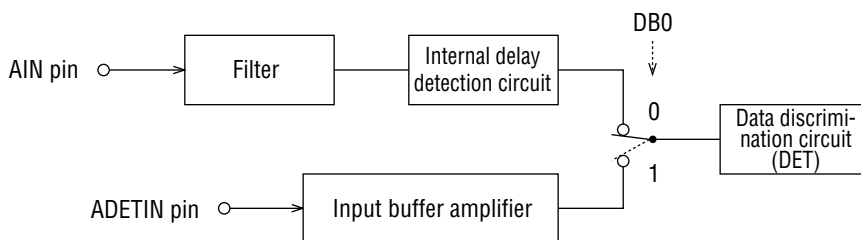


Figure 5.8.1 Switching Analog Input Pins

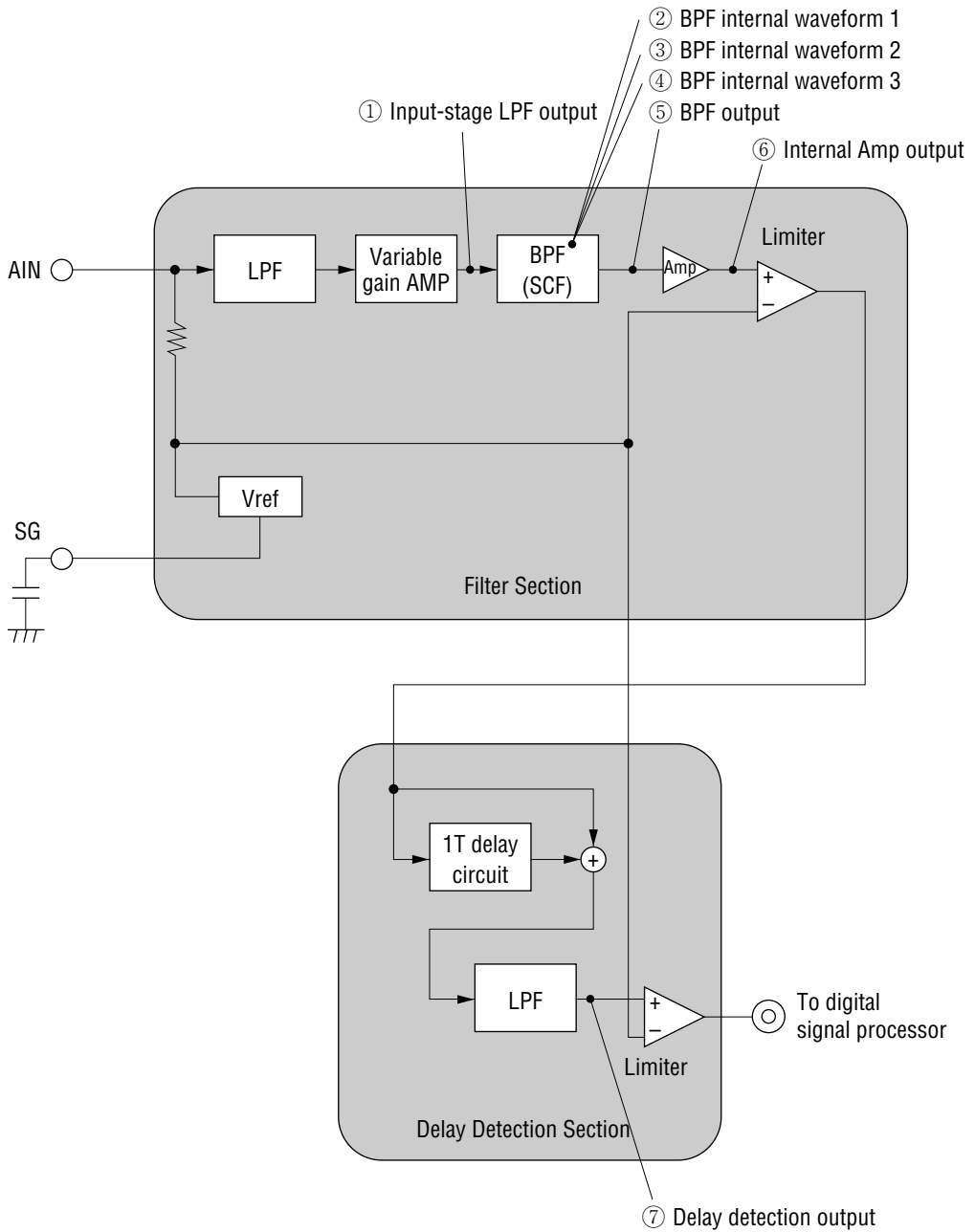
- (2) DB1-DB2: SGAIN0, SGAIN1  
This register is used for gain switching for the variable gain amplifier for analog input signal. These signals are used for initial settings.
- Set the values of DB1 and DB2 so that the following expression is satisfied:
- $$\text{Peak value of the analog input signal (composite signal)} \times \text{gain} = 1.5 \text{ to } 2.0 \text{ V}_{\text{P-P}} \text{ (MSM9552)}$$
- $$= 0.5 \text{ to } 0.9 \text{ V}_{\text{P-P}} \text{ (MSM9553)}$$
- This is effective for improving the S/N ratio.

| SGAIN1 | SGAIN0 | Gain  |
|--------|--------|-------|
| DB2    | DB1    |       |
| 0      | 0      | × 1   |
| 0      | 1      | × 1.5 |
| 1      | 0      | × 2   |
| 1      | 1      | × 3   |

(3) DB3-DB5: M0-M2

Monitors internal filter output waveforms and controls MON pin (pin 1) output. Refer to Figure 5.8.2 for the part that can be monitored. After clear, the internal MON amplifier is powered OFF and the output becomes high impedance.

| <b>(M2) DB5</b> | <b>(M1) DB4</b> | <b>(M0) DB3</b> | <b>MON Pin (pin 1) Output</b>                               |
|-----------------|-----------------|-----------------|---|
| 0               | 0               | 0               | Internal monitor amplifier power off, high impedance output |
| 0               | 0               | 1               | ① LPF output of input stage                                 |
| 0               | 1               | 0               | ② BPF internal waveform 1                                   |
| 0               | 1               | 1               | ③ BPF internal waveform 2                                   |
| 1               | 0               | 0               | ④ BPF internal waveform 3                                   |
| 1               | 0               | 1               | ⑤ BPF output  |
| 1               | 1               | 0               | ⑥ Internal amplifier output                                 |
| 1               | 1               | 1               | ⑦ Delay detection output                                    |



**Figure 5.8.2 Analog Section Output Waveform Monitor**



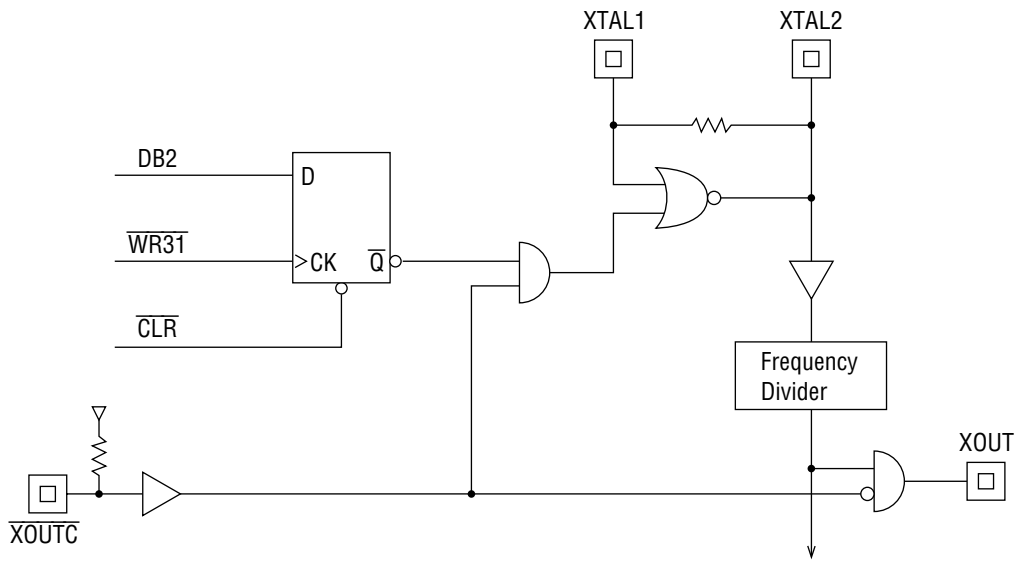
## 5.9 POWER DOWN CONTROL REGISTER

This is a power down setting register.

| Address | Read/write | Reset Value | (4) |     |     |     | (3) | (2) | (1) |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 031H    | Write      |             | —   | 0   | 0   | 0   | —   | 0   | 0   | 0   |

- (1) DB0: Analog section power down control  
 0: Power down (operation stops).  
 1: Power on (after power is turned on, several milliseconds are necessary until the circuit stabilizes).
- (2) DB1: Digital section power down control  
 0: The digital section is power down, and the internal clock stops. Since the clock stops at "H", operation can be continued after power on.  
 1: The digital section is power on. Operation starts from clock "H".
- (3) DB2: External oscillation control  
 When input pin  $\overline{XOUTC}$  = "1", operation of crystal oscillation circuits (XTAL1, XTAL2) is controlled as described below. The output pin XOUT is fixed to "L".  
 0: Stops the operation of the crystal oscillation circuits.  
 1: Starts the operation of the crystal oscillation circuits.  
 When input pin  $\overline{XOUTC}$  = "0", the crystal oscillation circuits (XTAL1 and XTAL2) are always in an oscillation state, and the output pin XOUT always outputs oscillation clocks.
- (4) Dividing of external clock (XOUT)  
 The divided clocks to the XOUT pin are set up.

| DB6<br>(XCK2) | DB5<br>(XCK1) | DB4<br>(XCK0) | Clock XOUT pin |
|---------------|---------------|---------------|----------------|
| 0             | 0             | 0             | 8.192 MHz      |
| 0             | 0             | 1             | 4.096 MHz      |
| 0             | 1             | 0             | 2.048 MHz      |
| 0             | 1             | 1             | 1.024 MHz      |
| 1             | 0             | 0             | 0.512 MHz      |
| 1             | 0             | 1             | 0.256 MHz      |
| 1             | 1             | 0             | 0.128 MHz      |
| 1             | 1             | 1             | 0.064 MHz      |



**Figure 5.9.1 Oscillator Circuit Control**

## 5.10 TEST CONTROL REGISTERS

### 5.10.1 Test Control 0

This register controls switching of the test pins (MOUT0-MOUT4).

| Address | Read/write | Reset value | (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 032H    | Write      |             | 0   | 0   | 0   | —   | —   | —   | —   | —   |

(1) DB5-DB7: See Table 5.10.1 for details.

### 5.10.2 Test Control 1

This register controls the decoding mode of serial receive data and test switching.

| Address | Read/write | Reset value | (5) (1) (4) (3) (2) (1) |     |     |     |     |     |     |     |
|---------|------------|-------------|-------------------------|-----|-----|-----|-----|-----|-----|-----|
|         |            |             | DB7                     | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 033H    | Write      |             | —                       | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

(1) DB0, DB4: Serial receive data output  
Outputs serial receive data (serial receive data converted by the control in (3) to (5) below) to MOUT6 pin.  
The output data changes at the rising edge of a 16 kHz regeneration data clock (MOUT5 pin).

| DB4 | DB0 | MOUT 6 Pin Output                       |
|-----|-----|---|
| 0   | 0   | Fixed to "L"                            |
| 0   | 1   | Serial receive data after descrambling  |
| 1   | 0   | Serial receive data before descrambling |
| 1   | 1   |   |

- (2) DB1: 16 kHz regeneration data clock  
A 16 kHz regeneration data clock is output to the MOUT5 pin.  
0: MOUT5 Pin is fixed to "L".  
1: A 16 kHz regeneration data clock is output to the MOUT5 pin.
- (3) DB2: Differential decoding control  
0: Performs differential decoding to input data.  
1: Does not perform differential decoding. (In FM multiplex broadcast, differential decoding is not used, so use DB2 = "1".)
- (4) DB3: Descrambler (regeneration of dc component of data) control  
0: Descrambles input data other than BIC. (This is used for receiving FM multiplex broadcast.)  
1: Does not descramble. (This is used for testing.)

(5) DB5, DB6: Delay detector output control

| <b>DB6</b> | <b>DB5</b> | <b>Delay Detector Control<br/>(controls input data and<br/>data before 1T)</b> | <b>Purpose of Use</b>            |
|------------|------------|--|----------------------------------|
| 0          | 0          | ENOR   | FM multiplex broadcast reception |
| 0          | 1          | Through (data before 1T)   | For testing                      |
| 1          | 0          | EOR  |                                  |
| 1          | 1          |  |                                  |

**Table 5.10.1 Monitor Input/Output Pins**

**Test Control 0**

| Test Control |         |        | Address = 032H   |                                    |               |                |                |                |
|--------------|---------|--------|------------------|------------------------------------|---------------|----------------|----------------|----------------|
|              |         |        | (DB7, DB6, DB5)  |                                    |               |                |                |                |
| Pin Name     | Pin No. | I/O    | Extension Port   | LSI Internal Signal Monitor (Note) |               |                |                |                |
|              |         |        |                  | (110)<br>(101)<br>(000)            | TST0<br>(001) | TSTT1<br>(010) | TSTB0<br>(011) | TSTB1<br>(100) |
| MOUT0        | 8       | Output | OFH register DB0 | BPF limiter output                 | TS11          | FRCK0          | FSYNC *1       |                |
| MOUT1        | 9       | Output | OFH register DB1 | Delay detection output             | TS21          | FRCK1          | BSYNC *2       |                |
| MOUT2        | 10      | Output | OFH register DB2 | DET output                         | TS10          | FRCK2          | RAMOUT         | BIC0 *3        |
| MOUT3        | 11      | Output | OFH register DB3 | SCF clock output                   | GATE          | FRCK3          | BICDET2        | BIC1 *3        |
| MOUT4        | 12      | Output | OFH register DB4 | Fixed to "L"                       | PHCK1         | BCK            | BICDET         | BICDET1 *4     |

(Note) Since the LSI internal signal monitor is normally used for LSI device shipment inspection, the user does not have to use it, but the items \*1 to \*4 below can be monitored.

\*1 FSYNC → Frame synchronizing state

"0": out of shnchronizing

"1": synchronizing

\*2 BSYNC → Block synchronizing state

"0": out of shnchronizing

"1": synchronizing

\*3 BIC0, BIC1 → BIC number indication

|         |      |      |      |      |
|---------|------|------|------|------|
| BIC0    | 0    | 1    | 0    | 1    |
| BIC1    | 0    | 0    | 1    | 1    |
| BIC No. | BIC1 | BIC2 | BIC3 | BIC4 |

\*4 BICDET1 → BIC detection state

"0": detecting NG

"1": detecting OK

**Test Control 1**

| Pin Name | Pin No. | I/O    | Test control 1<br>Address = 033H |       |                         |              |  |   |   |
|----------|---------|--------|----------------------------------|-------|-------------------------|--------------|--|---|---|
|          |         |        | Test Control 1 DB1               |       | Test control 1 DB0, DB4 |              |  |   |   |
|          |         |        | 0                                | 1     | DB0                     | 0            | 1                                      | 0                                       | 1 |
|          |         |        | 0                                | 1     | DB4                     | 0            | 0                                      | 1                                       | 1 |
| MOUT5    | 13      | Output | Fixed to "L"                     | CK16K | X                       | —            | —                                      | —                                       |   |
| MOUT6    | 14      | Output | —                                | —     | X                       | Fixed to "L" | Serial receive data after descrambling | Serial receive data before descrambling |   |

## 5.11 I/O ADDRESS REGISTER

This register sets up an internal register address irrespective of pins A0 to A5.

The address set up by this register becomes valid when IOEN (DB7) is set to "1".

When  $\overline{CS} = "1"$  and  $\overline{IORD} = "0"$ , data in the internal register is output onto the data bus.

When  $\overline{CS} = "1"$  and  $\overline{IOWR} = "0"$ , data on the data bus is written in the internal register.

| Address | Read/write | Reset<br>value | (1) |     | (2) |     |     |     |     |     |   |
|---------|------------|----------------|-----|-----|-----|-----|-----|-----|-----|-----|---|
|         |            |                | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |   |
| 037H    | Write      |                | 0   | —   | 0   | 0   | 0   | 0   | 0   | 0   | 0 |

(1) DB7: IOEN

0: Address set up by this register is invalid.

1: Address set up by this register is valid as an internal address in the IC.

(2) DB0 - DB5:

Corresponds to external addresses A0 to A5.

## 5.12 EXTENDED PORT REGISTER

Data (B0 to B4) in this register is output to the monitor output pins MOUT0 to MOUT4 by writing 000xxxxx, 101xxxxx, or 110xxxxx to the port mode register (032H). Refer to the table 5.10.1.

| Address | Read/write | Reset value | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---------|------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 00FH    | Write      |             | —   | —   | —   | 0   | 0   | 0   | 0   | 0   |

Usage example of the extended port

When the clock of the microcomputer that controls the MSM9552/9553 is supplied from the XOUT pin of the MSM9552/9553, the following two problems will occur:

1. When used with  $\overline{XOUTC} = "1"$

When this register is cleared, the microcomputer does not operate, because the XOUT pin is fixed at "L".

2. When used with  $\overline{XOUTC} = "0"$

When this register is cleared, oscillation does not stop even in the power down mode, because the XOUT pin always outputs clock.

The above troubles are cleared up using the extended port function.

By connecting the  $\overline{XOUTC}$  pin and MOUT0 pin externally as shown below,  $\overline{XOUTC}$  goes to "0" and XOUT pin outputs the clock, after clear.

By writing DB0 of 00FF to "1",  $\overline{XOUTC}$  is set to "1", during power down mode.

As a result, oscillation does not stop during clear, and can be stopped by the software only during power down mode.

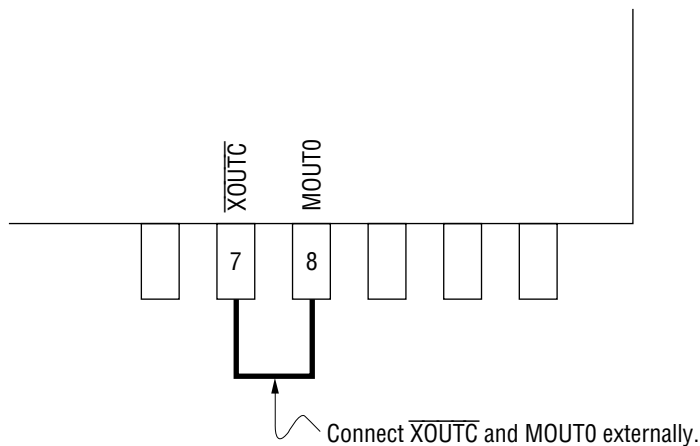


Figure 5.12.1 Usage Example of Extended Port



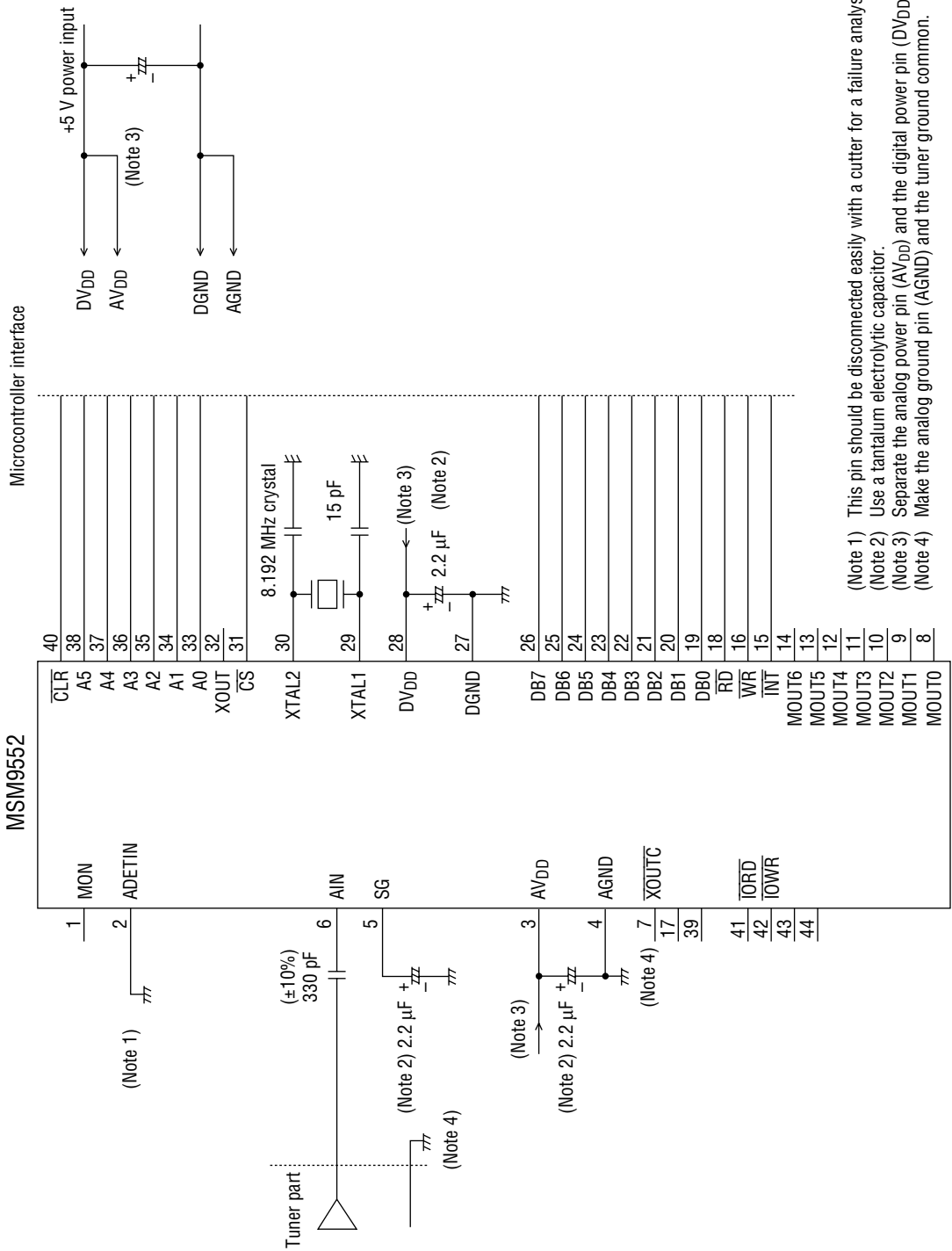


## *Chapter 6*

# EXTERNAL CONNECTION EXAMPLE

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## 6. EXTERNAL CONNECTION EXAMPLE



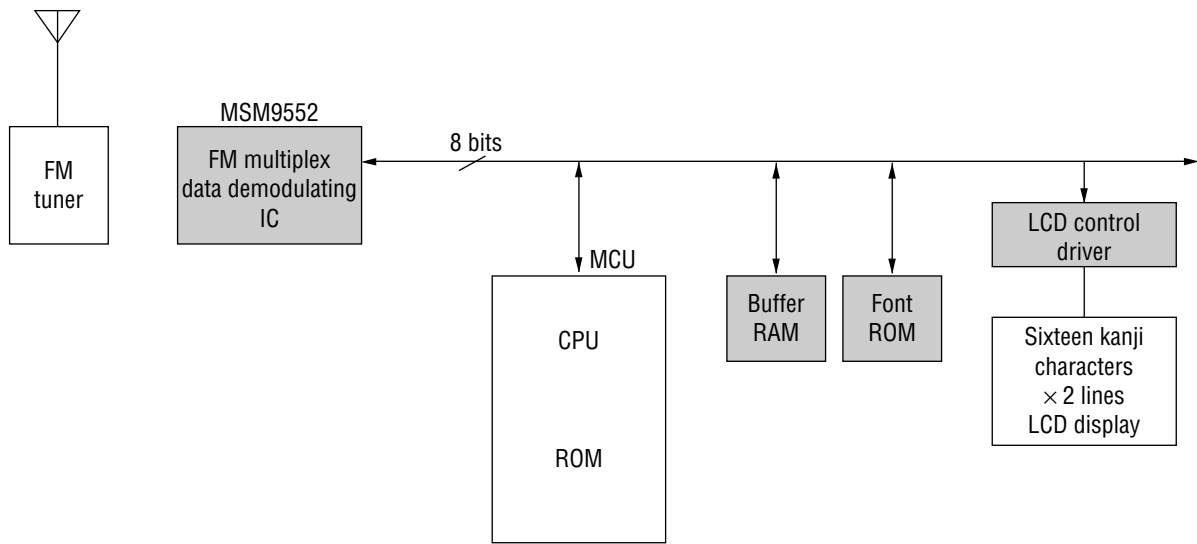


## ***Chapter 7***

# **APPLICATION CIRCUIT**

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7. APPLICATION CIRCUIT



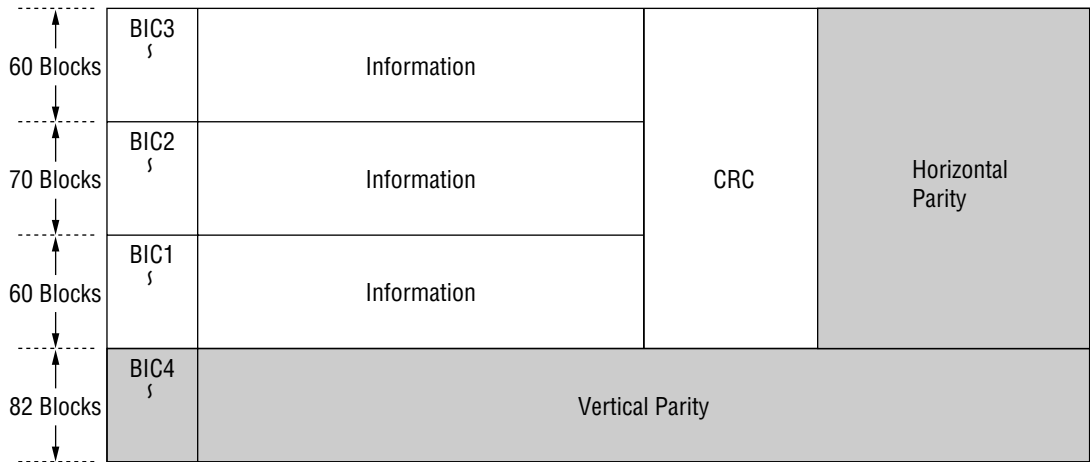


# APPENDIX

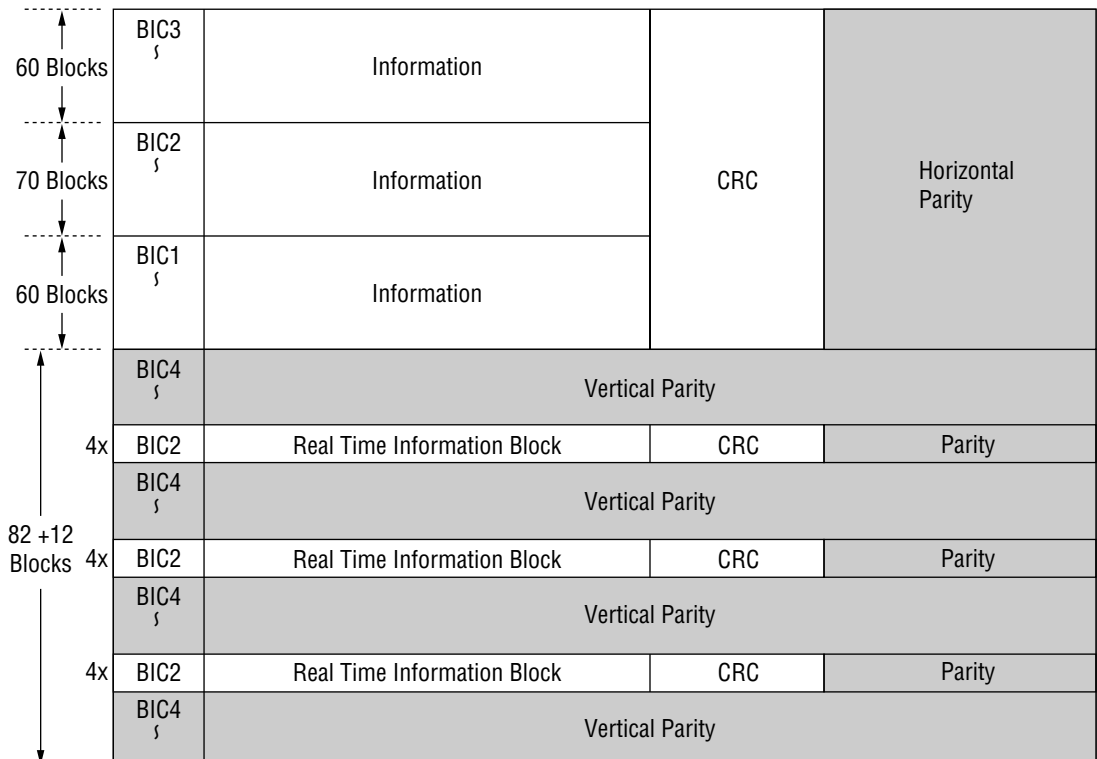
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## APPENDIX: INTERNATIONAL FRAME FORMAT (ITU-R Rec. BS1194)

1) Format A0: Frame according to method A, without insertion of real time blocks.



2) Format A1: Frame according to method A, with Static insertion of real time blocks.





3) Format B: Frame according to method B, with block interleave.

|            |           |                 |                |        |
|------------|-----------|-----------------|----------------|--------|
| 13 Blocks  | BIC1      | Information 1   | CRC            | Parity |
|            | ⋮         | ⋮               | ⋮              | ⋮      |
|            | BIC1      | Information 13  | CRC            | Parity |
| 123 Blocks | BIC3      | Information 14  | CRC            | Parity |
|            | BIC3      | Information 15  | CRC            | Parity |
|            | BIC4      | Parity 1        |                |        |
|            | BIC3      | Information 16  | CRC            | Parity |
|            | BIC3      | Information 17  | CRC            | Parity |
|            | BIC4      | Parity 2        |                |        |
|            | BIC3      | Information 18  | CRC            | Parity |
|            | ⋮         | ⋮               | ⋮              | ⋮      |
|            | BIC4      | Parity 40       |                |        |
|            | BIC3      | Information 95  | CRC            | Parity |
|            | BIC3      | Information 96  | CRC            | Parity |
|            | BIC4      | Parity 41       |                |        |
|            | 13 Blocks | BIC2            | Information 97 | CRC    |
| ⋮          |           | ⋮               | ⋮              | ⋮      |
| BIC2       |           | Information 109 | CRC            | Parity |
| 123 Blocks | BIC3      | Information 110 | CRC            | Parity |
|            | BIC3      | Information 111 | CRC            | Parity |
|            | BIC4      | Parity 42       |                |        |
|            | BIC3      | Information 112 | CRC            | Parity |
|            | BIC3      | Information 113 | CRC            | Parity |
|            | BIC4      | Parity 43       |                |        |
|            | BIC3      | Information 114 | CRC            | Parity |
|            | ⋮         | ⋮               | ⋮              | ⋮      |
|            | BIC4      | Parity 81       |                |        |
|            | BIC3      | Information 189 | CRC            | Parity |
|            | BIC3      | Information 190 | CRC            | Parity |
|            | BIC4      | Parity 82       |                |        |

4) Format C: Frame according to method C, block code only.

|      |             |     |        |
|------|-------------|-----|--------|
| BIC3 | Information | CRC | Parity |
|------|-------------|-----|--------|