OKI

MSM9563
IC for FM Multiplex Data Demodulation

User's Manual [Hardware]

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In the DARC system, 16kbps of digital data L-MSK modulated at 76KHz are multiplied on an ordinary FM broadcast base band signal.
An FM multiplex demodulation LSI performs decoding of the digital data signal.

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Chapter 1

GENERAL DESCRIPTION

1. GENERAL DESCRIPTION

The MSM9563 is an IC which demodulates FM character multiplex signals in the DARC (DAta Radio Channel) format to acquire digital data. This IC operates at 3 V. In the DARC format, baseband signals at ordinary FM broadcasting frequencies are multiplexed with 16 kbps digital data which is L-MSK-modulated at 76 kHz.

The MSM9563 has a bandpass filter consisting of an SCF, frame synchronization circuit, and error correction circuit on a single chip.

They allow a system for acquisition of digital data to be easily constructed by externally mounting an FM receiver tuner, microcontroller for control, and memory for temporary storage of data.

The MSM9563, a FM multiplex demodulator, has a simple configuration, and is equipped with only necessary functions. By making changes to software for the external microcontroller, the MSM9563 meets the various requirements of FM multiplex broadcasting services to be offered in future.

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FEATURES

- Built-in two receive channels including main channel and sub-channel (one of two FM stations can be selected)
- Pin compatible with MSM9553 / MSM9555
- Internal frame memory enables automatic error correction.
- Built-in bandpass filter (SCF)
- Built-in block synchronization circuit and frame synchronization circuit
- The number of synchronization protecting steps can be set
- Regeneration of data clocks by digital PLL
- 1T delay detector
- Built-in error correcting circuit (Vertical/Horizontal)
- Built-in layer-4 and layer-2 CRC processing circuit
- International frame formats A (supporting a real time block), B, and C available
- Microcontroller parallel interface
- Clock output for external devices (64 kHz to 8.192 MHz selectable)
- Power source: 2.7 to 3.6 V
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM9563GA)

Chapter 2

BLOCK DIAGRAM

2. BLOCK DIAGRAM

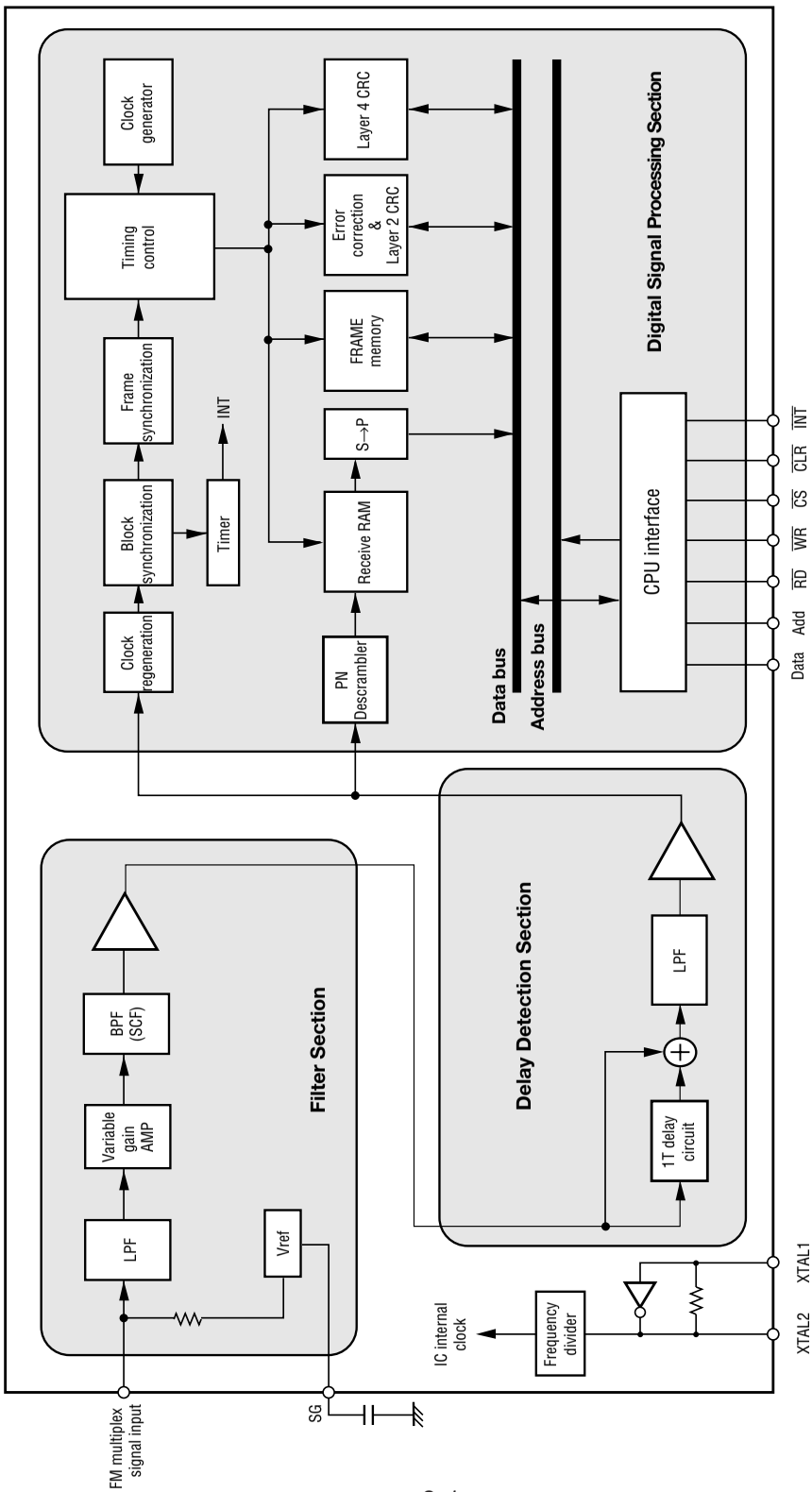


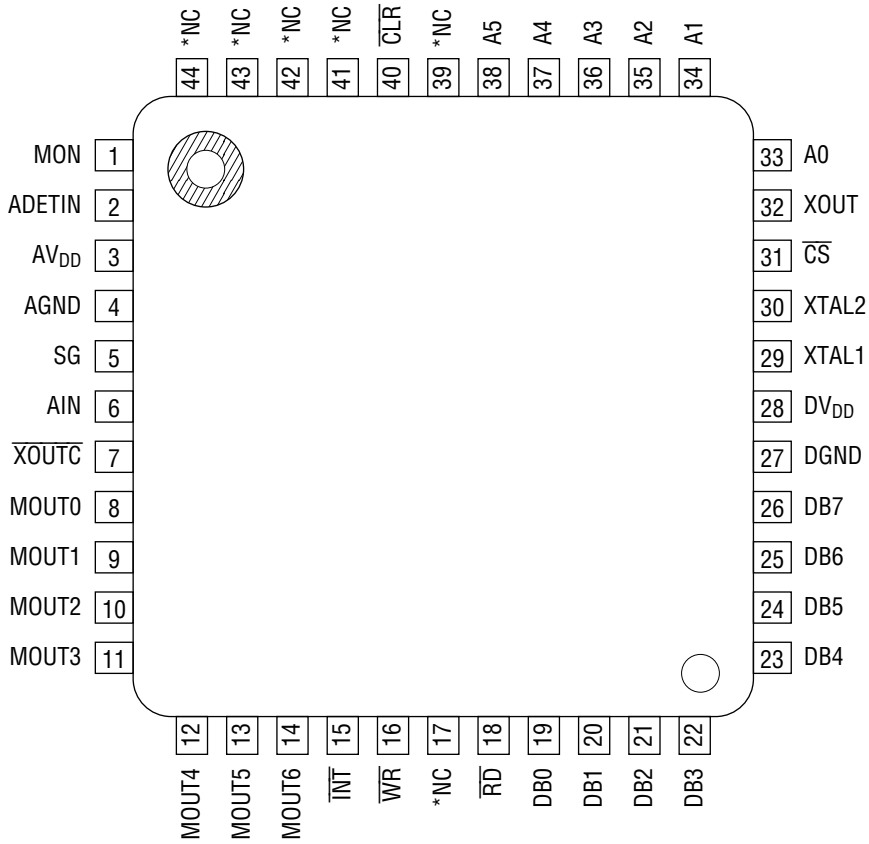
Figure 2.1 Block Diagram

Chapter 3

PIN INFORMATION

3. PIN INFORMATION

3.1 PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

Figure 3.1 Pin Layout

* Leave the NC pins (17, 39, 41, 42, 43, and 44) open.

3.2 PIN DESCRIPTIONS

Table 3.1 Pin Description

Function	Symbol	Pin	Type	Description
Microcontroller interface	$\overline{WR}$	16	I	Write signal to internal register.
	$\overline{RD}$	18	I	Read signal to internal register.
	$\overline{INT}$	15	O	Interrupt signal to microcontroller. When set to "L", an interrupt is generated.
	$\overline{CS}$	31	I	Chip select signal. When set to "L", the read, write, and data bus signals become effective.
	$\overline{CLR}$	40	I	When set to "L", the internal register is initialized, and the IC enters power down mode.
	A0 to A5	33 to 38	I	Address signal to internal register.
	DB0 to DB7	19 to 26	I/O	Data bus signal to internal register.
Tuner interface	AIN	6	I	FM multiple signal input.
	SG	5	O	Analog reference voltage pin. Connect a capacitor between this pin and the analog ground pin to prevent noise.
Analog section test	MON	1	O	Analog section waveform monitoring pin. The mode setting for the blocks in the analog section is specified by the analog section control register.
	ADETIN	2	I	Analog signal input pin for testing.
Digital section test	MOUT0 to MOUT6	8 to 14	O	Digital section test signal output and monitor output pins.
Clock	XTAL1	29	I	8.192 MHz crystal connection.
	XTAL2	30	O	8.192 MHz crystal connection.
	XOUT	32	O	Pin to supply variable clock (64 kHz to 8.192 MHz) to external devices.
	$\overline{XOUTC}$	7	I	XOUT control. "L" sets XOUT output, "H" sets XOUT output inhibit. This pin is pulled up internally.
Power supply	AV_{DD}	3	—	Analog power supply.
	AGND	4	—	Analog ground.
	DV_{DD}	28	—	Digital power supply.
	DGND	27	—	Digital ground.

Chapter 4

ELECTRICAL CHARACTERISTICS

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

No.	Parameter	Symbol	Condition	Rating	Unit
1	Power supply voltage	AV_{DD}	$AV_{DD} = DV_{DD}$ Ta = 25°C	–0.3 to +7.0	V
		DV_{DD}			
2	Input voltage	V_I		–0.3 to AV_{DD} + 0.3	
	Output voltage	V_O		–0.3 to DV_{DD} + 0.3	
3	Maximum power dissipation	P_D	Ta = 25°C, per package	400	mW
			Ta = 25°C, per output	50	
4	Storage temperature	T_{STG}	—	–55 to +150	°C

4.2 RECOMMENDED OPERATING CONDITIONS

No.	Parameter	Symbol	Condition	Range	Unit	Applied Pin
1	Power supply voltage	AV_{DD}	$AV_{DD} = DV_{DD}$	2.7 to 3.6	V	AV_{DD}
		DV_{DD}				DV_{DD}
2	Crystal oscillation frequency	f_{XTAL}	—	8.192 MHz ±100 ppm	—	XTAL1, XTAL2
3	FM multiplex signal input voltage	V_{AIN}*	Variable amplifier gain: × 1	0.6 to 0.9	V_{P-P}	AIN
			Variable amplifier gain: × 1.5	0.4 to 0.6		
			Variable amplifier gain: × 2	0.3 to 0.4		
			Variable amplifier gain: × 3	0.2 to 0.3		
4	Operating temperature	Ta	—	–40 to +85	°C	—

* Peak values (a total voltage of the following signals (a) to (c)) of composite signals including multiplex signals.
(a) Voice signals (100% modulated: voice max.)
(b) Pilot signal
(c) FM multiplex signals (10%: LMSK max.)
The maximum amplitude of an input signal is in the range of 0.9 V_{P-P} in which the internal IC circuit is not saturated.
Therefore, multiplex singnals of up to 0.9 V_{P-P} can be input if only multiplex signals (excluding composite signals) are input from a signal generator.

4.3 DC CHARACTERISTICS

(DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
1	Input voltage	V_{IH}	—	0.8 × DV_{DD}	—	—	V	$\overline{WR}$, $\overline{RD}$, $\overline{XOUTC}$, DB0 to DB7, $\overline{CS}$, A0 to A5, $\overline{CLR}$
		V_{IL}		—	—	0.2 × DV_{DD}		
2	Output voltage	V_{OH}	I_{OH} = –1 mA	DV_{DD} –0.5	—	—	V	MOUT0 to MOUT6, $\overline{INT}$, DB0 to DB7, XOUT
		V_{OL}	I_{OL} = 2 mA	—	—	0.45		
3	Input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	2	µA	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, DB0 to DB7, A0 to A5, $\overline{CLR}$
		I_{IL1}	V_{IL} = DGND	–2	—	—		
4	Input current 2	I_{IH2}	V_{IH} = AV_{DD}	—	—	2	µA	ADETIN
		I_{IL2}	V_{IL} = AGND	–2	—	—		
5	Input current 3	I_{IH3}	V_{IH} = DV_{DD}	—	—	2	µA	$\overline{XOUTC}$
6	Pull-up current	I_{pull}	DV_{DD} = 3 V, V_{IL} = DGND	3	15	50	µA	
7	Output off-leakage current	I_{OH}	V_{OH} = AV_{DD} During nonmonitoring (Hiz)	—	—	2	µA	MON
		I_{OL}	V_{OL} = AGND During nonmonitoring (Hiz)	–2	—	—		
8	Supply current	I_{DD}	During operation, no load f = 8.192 MHz	—	14	28	mA	AV_{DD}, DV_{DD}
			During power down, no load	—	—	50	µA	

4.4 AC CHARACTERISTICS

(DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C)

No.	Parameter	Symbol*	Condition	Min.	Typ.	Max.	Unit	Applied Pin
1	Write setup time	t_{SWR1}	See figure 4.1	3	—	—	ns	$\overline{WR}$, $\overline{CS}$, A0 to A5, DB0 to DB7
		t_{SWR2}	See figure 4.1	90	—	—		
2	Write hold time	t_{HWR1}	See figure 4.1	–18	—	—	ns	$\overline{WR}$, $\overline{CS}$, A0 to A5, DB0 to DB7
		t_{HWR2}	See figure 4.1	10	—	—		
3	Write pulse width	t_{WWR}	See figure 4.1	90	—	—	ns	$\overline{WR}$
4	Read setup time	t_{SRD}	See figure 4.2	3	—	—	ns	$\overline{RD}$, $\overline{CS}$, A0 to A5
5	Read hold time	t_{HRD}	See figure 4.2	–18	—	—	ns	$\overline{RD}$, $\overline{CS}$, A0 to A5
6	Read pulse width	t_{WRD}	See figure 4.2	90	—	—	ns	$\overline{RD}$
7	Read data output delay (1)	t_{DRD1}	See figure 4.2	—	—	90	ns	$\overline{RD}$, DB0 to DB7
8	Read data output delay (2)	t_{DRD2}	See figure 4.2	—	—	20	ns	$\overline{RD}$, DB0 to DB7
9	Layer 4 data Interval between write and write	t_{IWRWR2}	Layer 4 CRC mode See figure 4.3	620	—	—	ns	$\overline{WR}$
10	Layer 4 data Interval between write and read	t_{IWRRD1}	Layer 4 CRC mode See figure 4.3	1.2	—	—	µs	$\overline{WR}$, $\overline{RD}$
11	Interval between write and write	t_{IWRWR}	See figure 4.4	300	—	—	ns	$\overline{WR}$
12	Interval between write and write	t_{IWRWR1}	Continuously writing 0x3B to 0x3D to the same address See figure 4.5	550	—	—	ns	$\overline{WR}$
13	Interval between write and read	t_{IWRRD}	See figure 4.4	300	—	—	ns	$\overline{WR}$, $\overline{RD}$
14	Interval between read and read	t_{IRDRD}	See figure 4.6	300	—	—	ns	$\overline{RD}$
15	Interrupt CLR delay	$t_{DINTCLR}$	See figure 4.7	200	—	—	ns	$\overline{INT}$, $\overline{WR}$
16	CLR pulse width	t_{WCLR}	See figure 4.8	200	—	—	ns	$\overline{CLR}$

* See "TIMING DIAGRAM".

4.5 FILTER CHARACTERISTICS

(DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
1	BPF pass band attenuation	GAIN1	72 to 80 kHz Variable gain amplifier gain: 0 dB	—	—	3.0	dB	MON
2	BPF block band attenuation (1)	GAIN2	0 to 53 kHz Variable gain amplifier gain: 0 dB	50	—	—	dB	MON
3	BPF block band attenuation (2)	GAIN3	100 to 500 kHz Variable gain amplifier gain: 0 dB	50	—	—	dB	MON

4.6 TIMING DIAGRAM

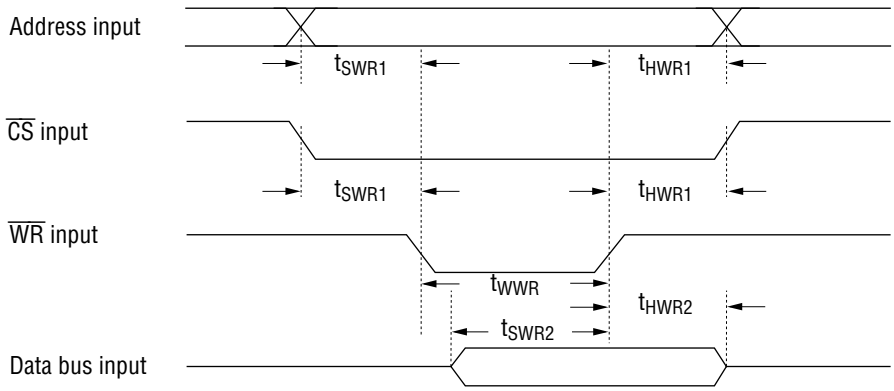


Figure 4.1 Write Timing

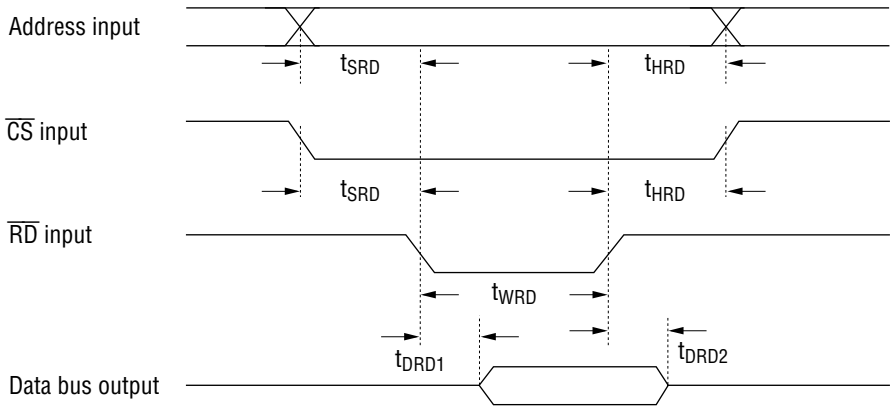


Figure 4.2 Read Timing

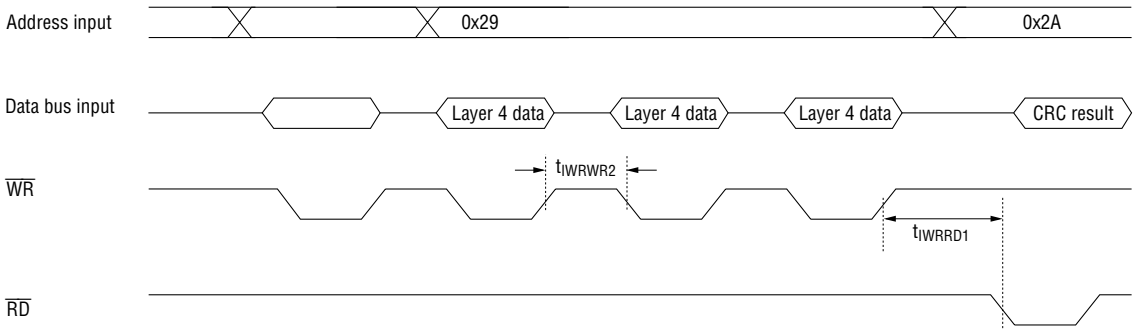


Figure 4.3 Layer 4 CRC mode and Layer 4 VICS mode Timing

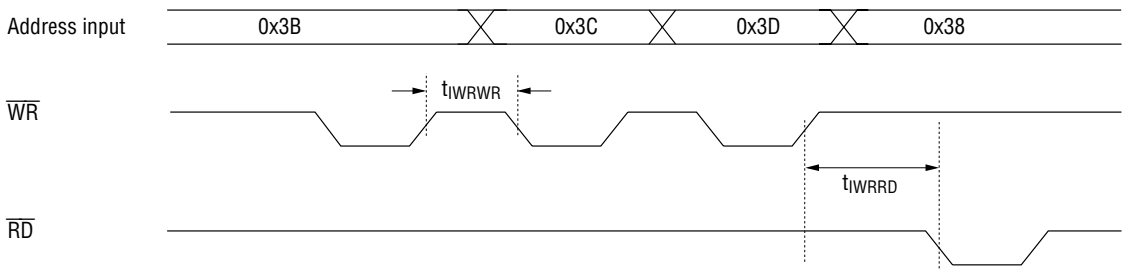


Figure 4.4 Internal between write and write or between write and read

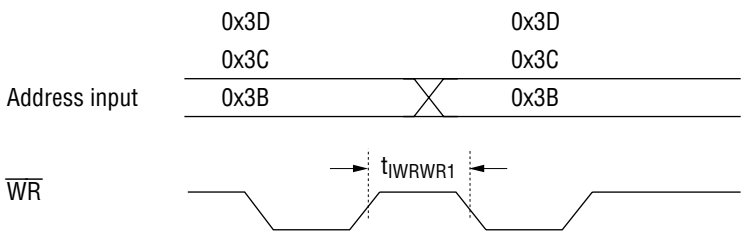


Figure 4.5 When 0x3B to 0x3D are continuously written at the same address (This is a rare case)

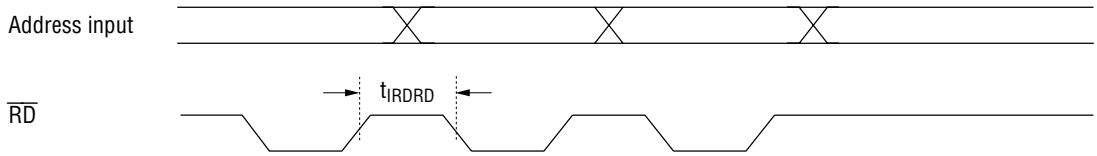


Figure 4.6 Intarval between read and read

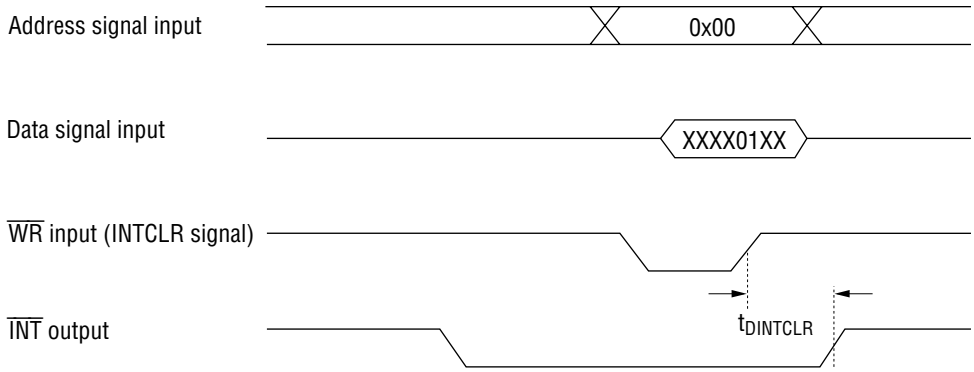


Figure 4.7 Interrupt CLR Timing

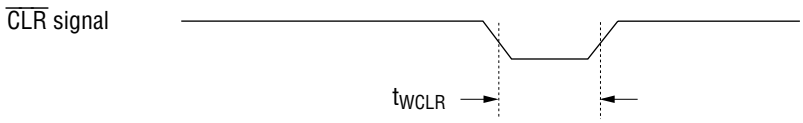


Figure 4.8 Clear pulse width

Chapter 5

CONTROL REGISTERS

5. CONTROL REGISTERS

5.1 OPERATING MODE REGISTERS

5.1.1 Mode setting of main channel and subchannel

Table 5.1.1 Main channel mode and subchannel mode

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x04	W	—	—	—	MOD_SUB	—	—	—	MOD_MAIN
	Initial value	—	—	—	0	—	—	—	1

There are two modes available, namely, the main channel mode in which connection is made to the broadcasting station of the same channel and reception is made in units of a frame (the conventional method), and the subchannel mode in which the tuner is switched intermittently to other channels and reception is made in units of several packets of information.
The channel switching mode setting for simultaneously receiving subchannels by switching to high speed subchannel during main channel reception is shown in the following table.

Channel switching mode setting for simultaneous reception of main channel and subchannels.

Mode	Set value		Description
	DB4	DB0	
MOD_MAIN/SUB	1	1	The mode used for subchannel timing extraction (at the time of initial setting).
MOD_MAIN	0	1	Main channel reception mode
MOD_SUB	1	0	Subchannel reception mode
MOD_OFF	0	0	The mode used for isolating the synchronization circuit after tuner switching until the tuning becomes stable.

5.1.2 Frame format

Table 5.1.2 Frame format

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x1F	W	—	—	—	—	—	—	B1	B0
	Initial value	—	—	—	—	—	—	1	0

Set value		Frame configuration	Symbol	Remarks
DB1	DB0			
0	0	Format A	A0	
0	1		A1	Includes real time information blocks
1	0	Format B	B	Used in Japan
1	1	Format C	C	

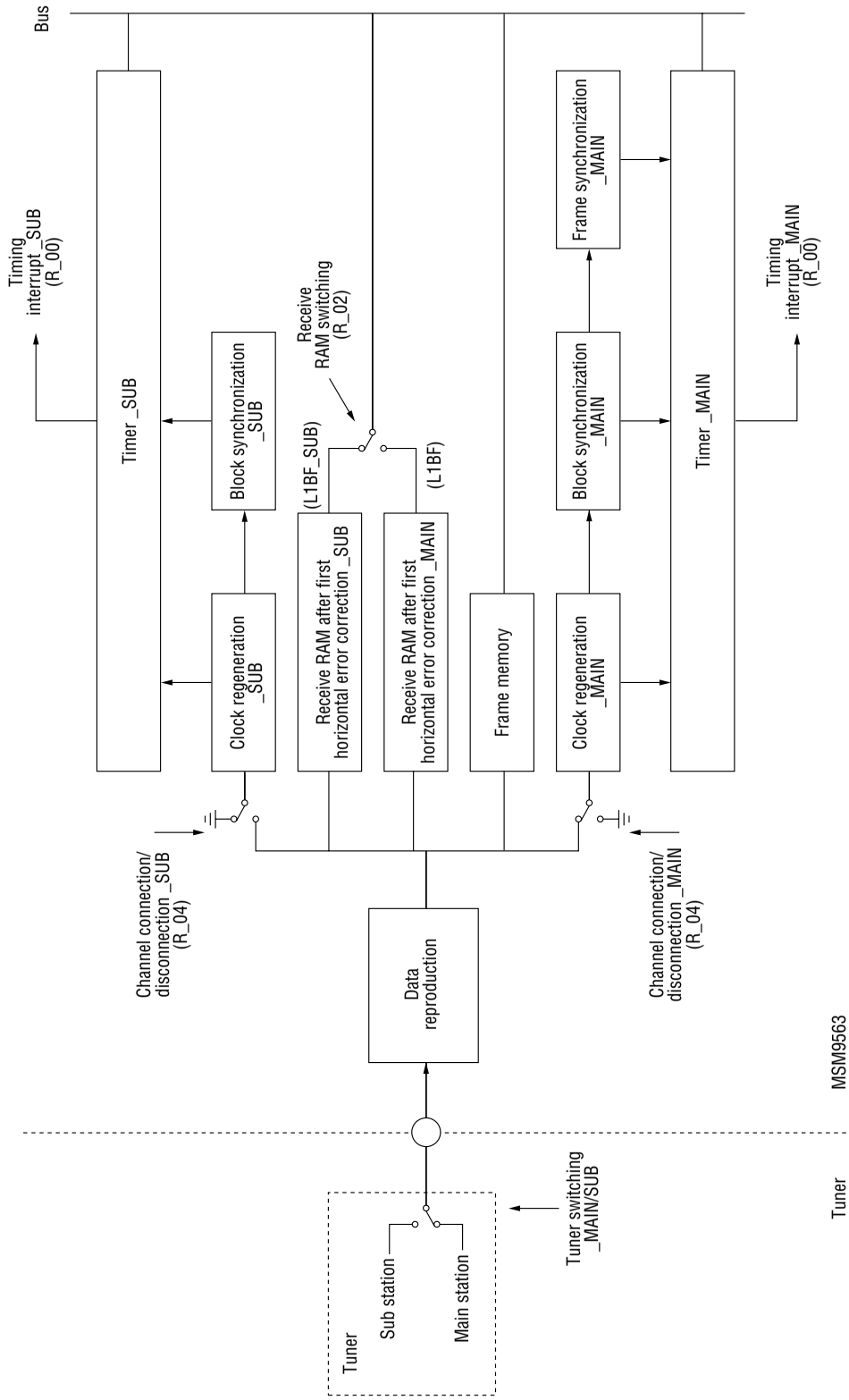


Figure 5.1 Main/Subchannel switching receive block diagram

5.1.3 Page mode

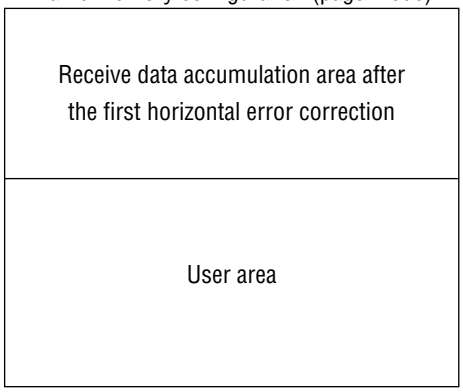
Table 5.1.3 Page mode

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x3E	W (Note)	—	MAINCH_CLRB	—	MOD_PARITERC2	CLRMC0_PAGE	MOD_PAGE	PAGE1	PAGE0
	Initial value	—	0	—	0	0	0	0	0

Note: The settings MOD_SUB=1 and MOD_MAIN=0 should be made in the register 0x04.

By setting the page mode, it is possible to automatically accumulate the received data after the first horizontal error correction in the frame memory. However, the frame synchronization, vertical error correction, and the second horizontal error correction are not made in the page mode.
The frame memory can be divided into the receive data accumulation area after first horizontal error correction and the user area, and the sizes of the two areas are variable.
DB3: The received packets are written startig from the packet address "0" if CLRMC0_PAGE is set to "1".

Frame memory configuration (page mode)

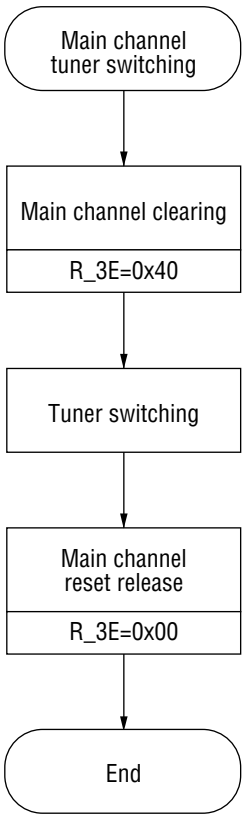


Receive data accumulation area after the first horizontal error correction and user area

Register 0x3E set value	Receive data accumulation area after the first horizontal error correction	User area
0x04	Packets 0 to 31	Packets 32 to 272
0x05	Packets 0 to 63	Packets 64 to 272
0x06	Packets 0 to 127	Packets 128 to 272
0x07	Packets 0 to 271	Not present

5.1.4 Main channel clear bit (MAINCH_CLRB)

This MAINCH_CLRB bit (DB6 of register 0x3E) has been provided to speed up switching to the main channel. When this bit is set to "1" (MAINCH_CLRB, BIT 6 =1), the main channel synchronization, error correction, internal frame memory control section, and interrupt will be reset.
However, the parameter setting registers, the counter for synchronization, and the pointer for reading out the frame memory are not cleared. Since the reset condition is retained, after switching the tuner, reset this bit to "0" (MAINCH_CLRB, DB6=0) thereby releasing the reset condition.
Thereafter, reception starts even if the register is not set again.
Although the frame memory is not cleared, the new receive data will be written over the old ones.



5.2 INTERRUPT REGISTERS

5.2.1 Interrupt register

When an interrupt occurs, a "1" is written in this register and the $\overline{INT}$ Pin is set to the "0" level. After reading out this register, write a "1" in the corresponding bit of this register to clear the interrupt.

Table 5.2.1 Interrupt register

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x00	R	Receive interrupt after the first horizontal error correction _SUB	TIMINT_ SUB	TIMINT_ MAIN	Receive interrupt after the second horizontal error correction	—	Out-of-synchronization interrupt	Receive interrupt after the first horizontal error correction _MAIN	REAL Packet
	W	Clear interrupt	Clear interrupt	Clear interrupt	Clear interrupt	—	Clear interrupt	Clear interrupt	—
	Initial value	0	0	0	0	—	0	0	0

(1) DB7: Receive interrupt after the first horizontal error correction_SUB

1: Indicates that a packet was received in a subchannel.
0: There is no interrupt in the subchannels.

(2) DB6: TIMINT_SUB

1: Indicates that an interrupt set by the subchannel timer has occurred.
0: There is no interrupt in the subchannels.

(3) DB5: TIMINT_MAIN

1: Indicates that an interrupt set by the main channel timer has occurred.
0: There is no interrupt in the main channel.

Settings of the registers 0x05, 0x16, 0x17, 0x1D, and 0x1E are necessary to activate the main channel timer interrupt.

(4) DB4: Receive interrupt after the second horizontal error correction

1: Indicates that an interrupt of the frame data reception after the second horizontal error correction of the main channel has occurred.
0: There is no interrupt in the main channel.

(5) DB2: Out-of-synchronization interrupt

1: Indicates that an interrupt of frame out-of-synchronization has occurred.
0: There is no interrupt in the main channel.

(6) DB1: Receive interrupt after the first horizontal error correction_MAIN

1: Indicates that a packet was received in the main channel.
0: There is no interrupt in the main channel.

(7) DB0: REAL

This bit is not an interrupt.
This bit is cleared simultaneously with the receive interrupt after the first horizontal error correction _MAIN when a "1" is written in DB1.

1: Indicates that the received packet is a REAL packet.
0: The received packet is not a REAL packet.

5.2.2 Interrupt mask

This is a register that controls the interrupts corresponding to the bit numbers of the interrupt register (0x00).

Table 5.2.2 Interrupt mask

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x01	W	Interrupt mask	Interrupt mask	Interrupt mask	Interrupt mask	—	Interrupt mask	Interrupt mask	—
	Initial value	0	0	0	0	—	0	0	—

1: Interrupt enabled.
0: Interrupt disabled.

5.3 RECEIVE DATA REGISTERS

When data is received, that fact is reported by generating an interrupt and setting the $\overline{INT}$ pin to the "0" level, after which the received data should be read out from the receive data port. The receive data ports are the recive port (0x03) after first horizontal error correction from which data should be read out in units of a packet after the first horizontal error correction has been completed, and the receive port (0x38) after second horizontal error correction from which data can be read out in units of a frame after the second horizontal error correction has been completed.

Receive port after the first horizontal error correction
Since the receive port after the first horizontal error correction is internally separated into one for the main channel and one for the subchnnel, it is necessary to select the required port before reading data. The receive data interrupt after the first horizontal error correction can be set to be enabled or disabled according to the conditions of parity packet, error correction result, service identifier, etc.

Receive port after the second horizontal error correction
The receive data of the receive port after the second horizontal error correction is reported by an interrupt at the timing of the 13th packet of the next frame. When all the packets of the frame have been received, the vertical error correction would have been completed. However, the vertical error correction would have been omitted when all the packets in the frame have not been received, such as when frame synchronization is entered in the middle of a frame. The second horizontal error correction is carried out for the packet received under frame synchronization and its result is indicated in register 0x37 by dividing it into four groups as the frame synchronization condition.
The test settings described later are necessary for reading the received data including the parity packet, and in this case, the reception is reported by an interrupt generated at the timing of the 15th packet. Before reading data from the receive port after the second horizontal error correction, it is necessary to set the address pointer (0x3B to 0x3D) and the access mode (0x39) of the frame memory. The address pointer consists of the packet number and the byte number, and specifies the starting address of reading. The setting of the access mode consists of setting the modes of horizontal/vertical reading direction, the parity read, etc., of the frame memory.
The frame data (for example, 190x24 bytes) of the receive port after the second horizontal error correction can be read out either successively or intermittently.

5.3.1 Switching the receive port after the first horizontal error correction

Table 5.3.1 Switching the receive port after the first horizontal error correction

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x02	W	—	—	—	—	—	—	—	MAINB/ SUB
	Initial value	—	—	—	—	—	—	—	0

Since the receive port after the first horizontal error correction is connected to the 36-byte RAM for the main channel (LIBF) and the RAM for the subchannel (LIBF_SUB) (see Figure 5.1), it is necessary to switch between them according to the content of the receive interrupt register. When a value is set in this register, the RAM address pointer is reset and it is possible to read from the leading byte.

DB0: MAINB/SUB

1: The receive port after the first horizontal error correction is connected to the RAM (LIBF_SUB) for the subchannel.
0: The receive port after the first horizontal error correction is connected to the RAM (LIBF) for the main channel.

5.3.2 Receive port after the first horizontal error correction and the receive data format

Table 5.3.2.1 Receive port after the first horizontal error correction

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x03	R	B7	B6	B5	B4	B3	B2	B1	B0
	W	B7	B6	B5	B4	B3	B2	B1	B0
	Initial value	—	—	—	—	—	—	—	—

Read
This is the one-packet receive data port after the first horizontal error correction. The read address of the internal RAM is "0x00" when a receive interrupt after the first horizontal error correction has occurred. When this port is read, the read address is automatically incremented to the next read address and hence it is possible to carry out successive reads.

Write
For testing only. Writing to this port is prohibited during normal use.

Table 5.3.2.2 Receive data format after the first horizontal error correction

		Bit No.							
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Byte No.	BYTE0	CRC0	ERC0	RECCRC	FSYNC	BSYNC	BICDET	BIC1	BIC0
	BYTE1	VICSRDY	PARITY	INT0	0	0	FNCHG	FRNO1	FRNO0
	BYTE2	First horizontal correction receive data No. 0							
	:	:							
	:	:							
	BYTE23	First horizontal correction receive data No. 21							
	BYTE24	CRC							
	BYTE25	PARITY		CRC					
	BYTE26	PARITY							
	:	:							
	BYTE35	PARITY							

BYTE0 and BYTE1 of the receive RAM data after the first horizontal error correction indicate the status of the received packet, BYTE2 to BYE23 are data, and BYTE 24 to BYTE 35 are the CRC/ parity data.
BYTE24 to BYTE35 are for testing and cannot be read out.

BYTE0

(1) DB7: CRC0

1: Indicates that there is an error in the CRC of the packet after the first horizontal error correction.
0: Indicates that the CRC of the packet is normal after the first horizontal error correction.

(2) DB6: ERC0

1: Indicates that there is an error in the correction result of the packet after the first horizontal error correction.
0: Indicates that the correction result of the packet is normal after the first horizontal error correction.

(3) DB5: RECCRC

1: Indicates that there is an error in the CRC of the received packet before error correction.
0: Indicates that the CRC of the received packet is normal before error correction.

(4) DB4: FSYNC

1: Indicates that the received packet is in a frame synchronization state.
0: Indicates that the received packet is in a frame out-of-synchronizaiton state.

(5) DB3: BSYNC

1: Indicates that the received packet is in a block synchronization state.
0: Indicates that the received packet is in a block out-of-synchronization state.

(6) DB2 to DB0: BIC Data

Indicate the detection condition of the block identification code (BIC).

DB2	DB1	DB0	BIC No.
1	0	0	1
1	0	1	2
1	1	0	3
1	1	1	4
0	—	—	Not detected

BYTE1

(1) DB7: VICSRDY

1: Indicates that the received packet is a VICS packet.
0: Indicates that the received packet is not a VICS packet.

(2) DB6: PARITY

This bit indication is made only in a frame synchronization state.
1: Indicates that the received packet is a parity packet.
0: Indicates that the received packet is not a parity packet.

(3) DB5: INT0

This bit indicates the receive interrupt after the first horizontal error correction. Even though this bit indication is made in the reception condition after the second horizontal correction, it is possible to confirm that reading has been made when a receive interrupt has occurred after the first horizontal error correction.

1: Indicates that the received packet is one in which the receive interrupt occurred after the first horizontal error correction.
0: Indicates that the received packet is one in which no receive interrupt occurred after the first horizontal error correction.

(4) DB4, DB3: "0" fixed

(5) DB2: FNCHG

This bit indication is made only in a frame synchronization state.

1: Indicates that the packet is one given in the following table.
0: Indicates that the packet is one other than those indicated in the following table.

Frame format	
Format B	Format A1, A0
Packet with a block number of 0, 13, 136, or 149.	Packet with a block number of 0, 60, 130, or 190.

Note: The packet numbers are expressed in this manual as 0 to 271 (A1: 0 to 283).

(6) DB1, DB0: FRNO1, FRNO0

These bit indications are made only in a frame synchronization state.
These bits indicate that the packet is one with the block numbers given in the following table.

DB1	DB0	Frame format		
		Format B	Format A1, A0	
0	0	Packet with a block number of 0 to 12.	Packet with a block number of 0 to 59	
0	1	Packet with a block number of 13 to 135.	Packet with a block number of 60 to 129	
1	0	Packet with a block number of 136 to 148.	Packet with a block number of 130 to 189	
1	1	Packet with a block number of 149 to 271.	A0	Packet with a block number of 190 to 271
			A1	Packet with a block number of 190 to 283

Note: The packet numbers are expressed in this manual as 0 to 271 (A1: 0 to 283).

5.3.3 Conditions of receive interrupt after the first horizontal error correction

Table 5.3.3.1 Conditions of receive interrupt after the first horizontal error correction

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x34	W	MOD_ FSYNC	MOD_CH OFFDET	MOD_ INT0	MOD_ ERC0	MOD_ PARIT0	MOD_ BICDET0	MOD_ SI	SISEL
	Initial value	0	0	1	0	0	0	0	0

This is the register for setting the conditions of interrupt after the first horizontal error correction. During the initial setting, all packets received in a synchronization state are set to generate an interrupt. It is possible to specify the four types of interrupt conditions shown in the following table regarding good (error-free) packets, frame synchronization, and specified SI (service identifier). It is possible to specify 16 types of service identifiers (SI0 to SI15) for which it is necessary to set this register and the register 0x35.
The packets that generated an interrupt after the first horizontal error correction are recorded in the frame memory (Receiving state 1 DB5 (INT0)) after the second horizontal error correction. Therefore, there is no need to read out good packets after the first horizontal error correction after the second horizontal error correction.

Table 5.3.3.2 Interrupt conditions after the first horizontal error correction

	Interrupt condition	Set value of 0x34	Set value of 0x35
1	All packets received in a synchronization state	0x20	—
2	Good packets received in a synchronization state	0x70	—
3	Packets in a frame synchronization state (including bad packets)	0xA0	—
4	Good packets with the specified service identifier SI.	0x7A	SI0 to SI7 written in units of a bit
		0x7B	SI8 to SI15 written in units of a bit

5.3.4 Specification of SI (Service identifier)

Table 5.3.4 SI Specification

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x35	W (Note 1)	SI7	SI6	SI5	SI4	SI3	SI2	SI1	SI0
	W (Note 2)	SI15	SI14	SI13	SI12	SI11	SI10	SI9	SI8
	Initial value	1	1	1	1	1	1	1	1

Note 1: The setting SISEL=0 should have been made in the register 0x34.
Note 2: The setting SISEL=1 should have been made in the register 0x34.

This is the register for setting the service identifier SI which is an interrupt condition after the first horizontal error correction.
It is possible to specify multiple service identifiers by setting "1" to the bits corresponding to the required service identifiers among the 16 types SI0 to SI15 in the above table.

5.3.5 Receive port after the second horizontal error correction

Table 5.3.5 Receive data port after the second horizontal error correction

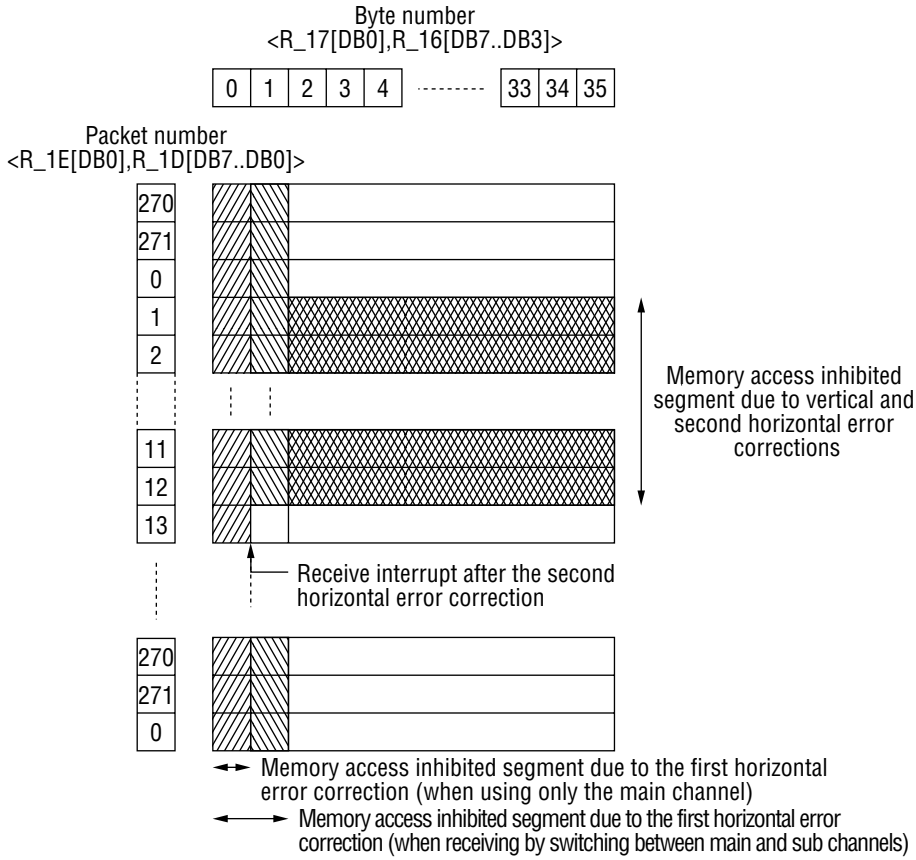
Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x38	R	B7	B6	B5	B4	B3	B2	B1	B0
	W	B7	B6	B5	B4	B3	B2	B1	B0
	Initial value	—	—	—	—	—	—	—	—

The receive port after the second horizontal error correction is connected to the frame memory. It is possible to read the frame memory successively since the frame memory address is incremented automatically whenever this port is read. It is also possible to read this port starting from any required address.
Packets in a frame synchronization state are accumulated in the frame memory. When the reception of one full frame is completed, the vertical error correction and the second horizontal error correction are made, and the receive interrupt after the second horizontal error correction occurs at the timing of the 13th packet in the next frame.
Although it is possible to receive from the middle of a frame, the vertical error correction will be omitted in that case. The frame synchronization state is indicated in the register 0x37 by dividing it into four groups. On the other hand, it is also possible to know this from the status indication byte at the beginning of each packet.
The volume of data in the frame memory is;
• 24x190 bytes in the case of 4-layer data including packet status indication;
• 36x273 bytes in the case of data including parity, etc.
See the data format of the receive frame memory after the second horizontal error correction in Section 5.3.6 for the detailed contents of data.

CAUTION: The frame memory has segments that are prohibited from being accessed. See Figure 5.3 for details.

Figure 5.3 Access prohibited segments of the frame memory (R_38)

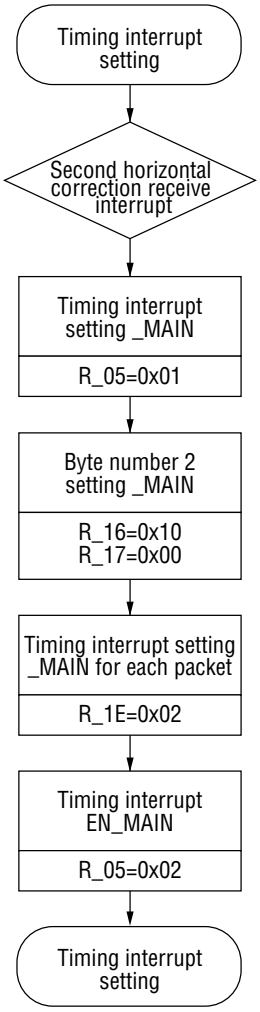
(1) The frame memory access inhibited time occurs when the intersection of the packet number and the byte number correspond to the hatched parts in the follwoing figure.
(2) It is possible to know the packet number and the byte number by reading out the registers R_1E, R_1D, R_16, and R_17. (See the precautions to be taken at the time of reading out the packet number and byte number given in the next page.)



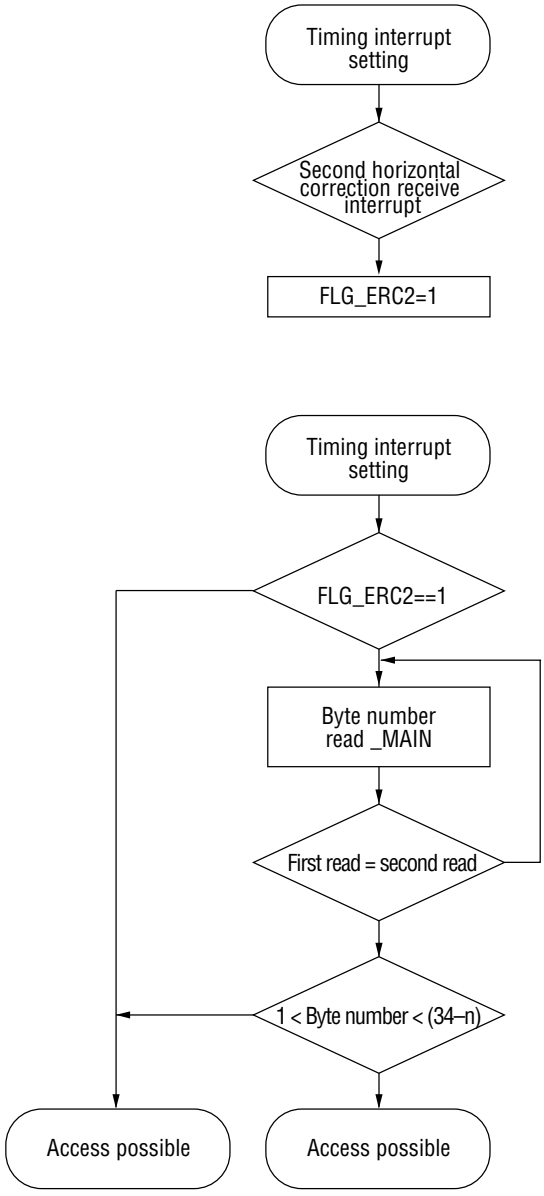
Precautions in reading the packet number and byte number

Since the microcontroller and data clocks are not mutually synchronized, it is possible that wrong values are read out when reading out is made when the packet number or the byte number is changing. Therefore, it is necessary to read them twice successively and use only after confirming that there is a match between the two successive values.

(1) Memory access is possible for about 16msec after the timing interrupt



(2) Checking the byte number and the packet number of Figure 5.3



n is the time of accessing the memory

5.3.6 Data configuration of the receive frame memory after the second horizontal error correction

Table 5.3.6.1 Receive frame memory data configuration after the second horizontal error correction

	Byte No.							
Packet No.	**0**	**1**	**2**	**· ·**	**23**	**24**	**· ·**	**35**
0	Reception status 0	Reception status 1	Data 0	· ·	Data 21	CRC/ PARITY	· ·	PARITY
:	:	:	:	:	:	:	:	:
189	Reception status 0	Reception status 1	Data 0	· ·	Data 21	CRC/ PARITY	· ·	PARITY
190	Reception status 0	Reception status 1	Vertical correction parity	Vertical correction parity	Vertical correction parity	Vertical correction parity	Vertical correction parity	Vertical correction parity
:	:	:	:	:	:	:	:	:
271	Reception status 0	Reception status 1	Vertical correction parity	Vertical correction parity	Vertical correction parity	Vertical correction parity	Vertical correction parity	Vertical correction parity
272	—	—	Vertical correction result 0	· ·	· ·	· ·	· ·	Vertical correction result 33

The frame memory data configuration is shown in Table 5.3.6.1. The data consists of 190 data packets, 82 parity packets, and one vertical correction result packet. Normally, the second horizontal error correction of the parity packets 190 to 271 are omitted. To read packets including the parity packets after the second horizontal error correction, it is necessary to set and carry out the error correction separately for testing purposes.
The leading two bytes of each packet indicate the reception status.
The details of the reception status are shown in Table 5.3.6.2.

Table 5.3.6.2 Reception status after the second horizontal error correction

	DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
Reception status 0	CRC0	ERC0	RECCRC	FSYNC	BSYNC	BICDET	BIC1	BIC0
Reception status 1	VICSRDY	PARITY	INT0	CRC2	ERC2	FNCHG	FRNO1	FRNO0

Reception status 0
The reception status 0 is equal to the contents of BYTE0 received after the first horizontal error correction.

(1) DB7: CRC0

1: Indicates that there is an error in the CRC of the packet after the first horizontal error correction.
0: Indicates that the CRC of the packet is normal after the first horizontal error correction.

(2) DB6: ERC0

1: Indicates that there is an error in the correction result of the packet after the first horizontal error correction.
0: Indicates that the correction result of the packet is normal after the first horizontal error correction.

(3) DB5: RECCRC

1: Indicates that there is an error in the CRC of the received packet before error correction.
0: Indicates that the CRC of the received packet is normal before error correction.

(4) DB4: FSYNC

1: Indicates that the received packet is in a frame synchronization state.
0: Indicates that the received packet is in a frame out-of-synchronizaiton state.

(5) DB3: BSYNC

1: Indicates that the received packet is in a block synchronization state.
0: Indicates that the received packet is in a block out-of-synchronization state.

(6) DB2 to DB0: BIC Monitor

Indicate the detection condition of the block identification code (BIC).

DB2	DB1	DB0	BIC No.
1	0	0	1
1	0	1	2
1	1	0	3
1	1	1	4
0	—	—	Not detected

Reception status 1
(1) DB7: VICSRDY

1: Indicates that the received packet after the second horizontal error correction is a VICS packet.
0: Indicates that the received packet after the second horizontal error correction is not a VICS packet.

(2) DB6: PARITY

This bit indication is made only in a frame synchronization state.
1: Indicates that the received packet is a parity packet.
0: Indicates that the received packet is not a parity packet.

(3) DB5: INT0

1: Indicates that the received packet is the one in which the receive interrupt occurred after the first horizontal error correction.
It is not necessary to read this if the reading has already been done during the reception after the first horizontal error correction.
0: Indicates that the received packet is one in which no receive interrupt occurred after the first horizontal error correction.

(4) DB4: CRC2

1: Indicates that there is an error in the CRC of the packet after the second horizontal error correction.
0: Indicates that the CRC of the packet is normal after the second horizontal error correction.

(5) DB3: ERC2

1: Indicates that there is an error in the correction result of the packet after the second horizontal error correction.
0: Indicates that the correction result of the packet is normal after the second horizontal error correction.

Note: CRC2=ERC2=0 is necessary for the packet to be good (error-free).

(6) DB2: FNCHG

This bit indication is made only in a frame synchronization state.
1: Indicates that the packet is one with a block number of 1, 14, 137, or 150 in the case of the frame format B, and with a block numaber of 1, 61, 131, or 191 in the case of the frame formats A0 and A1.
0: Indicates that the packet is one other than the above.

(7) DB1, DB0: FRNO1, FRNO0

These bit indications are made only in a frame synchronization state.
These bits indicate that the packet is one with the block numbers given in the following table.

DB1	DB0	Frame format		
		Format B	Format A1, A0	
0	0	Packet with a block number of 0 to 12.	Packet with a block number of 0 to 59	
0	1	Packet with a block number of 13 to 135.	Packet with a block number of 60 to 129	
1	0	Packet with a block number of 136 to 148.	Packet with a block number of 130 to 189	
1	1	Packet with a block number of 149 to 271.	A0	Packet with a block number of 190 to 271
			A1	Packet with a block number of 190 to 283

Note: The packet numbers are expressed in this manual as 0 to 271 (A1: 0 to 283).

5.3.7 Setting the receive frame memory access mode after the second horizontal error correction

Table 5.3.7 Frame memory access mode

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x39	W	BANK CONT1	BANK CONT0	VLBCNT	PCTL1 BL2	VBACK	LBACK1	LBACK0	LSTART
	Initial value	0	0	0	0	0	1	0	0

This is the register for setting the access mode so that reading can be done efficiently when reading the frame memory successively.

(1) DB7, DB6: BANK1, BANK0

These bits are for making settings for testing purposes. Normally use with the settings of DB7=DB6=0.

(2) DB5: VLBCNT

1: The frame memory is read in the vertical direction (in an ascending order of the packet number with the byte number being kept fixed).
0: The frame memory is read in the horizontal direction (in an ascending order of the byte number with the packet number being kept fixed).
The packet number is incremented by 1 when the byte number reaches that specified by LBACK0 and LBACK1.

(3) DB4: PCTL1BL2

The readable frame memory address (packet number) is selected from the registers 0x3C and 0x3D.
1: Enables the MSM9563 to read the address (packet number) of the receive data packet that is being written.
0: Enables an external microcontroller to read the address (packet number) of the receive data packet that is being accessed.

(4) DB3: VBACK

1: When the packet number becomes 272, the next packet number will be reset to 0. For testing purposes only.
0: When the packet number becomes 189, the next packet number will be reset to 0.

(5) DB2, DB1: LBACK1, LBACK0

The next byte number is reset to the byte number specified by LSTART when the current byte number becomes the returning byte number given in the following table.

LBACK1	LBACK0	Returning byte No.
0	0	1
0	1	2
1	0	23
1	1	35

(6) DB0: LSTART

1: The next byte number is reset to 2 when the current byte number becomes equal to the value specified by LBACK0 and LBACK1.
0: The next byte number is reset to 0 when the current byte number becomes equal to the value specified by LBACK0 and LBACK1.

5.3.8 Receive frame memory pointer after the second horizontal error correction

Table 5.3.8.1 Frame memory address (1/3)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x3B	R/W	—	—	EXT BYTE5	EXT BYTE4	EXT BYTE3	EXT BYTE2	EXT BYTE1	EXT BYTE0
	Initial value	—	—	0	0	0	0	0	0

Table 5.3.8.2 Frame memory address (2/3)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x3C	R (Note 1)	EXT PCT7	EXT PCT6	EXT PCT5	EXT PCT4	EXT PCT3	EXT PCT2	EXT PCT1	EXT PCT0
	R (Note 2)	L1BF PCT7	L1BF PCT6	L1BF PCT5	L1BF PCT4	L1BF PCT3	L1BF PCT2	L1BF PCT1	L1BF PCT0
	W	EXT PCT7	EXT PCT6	EXT PCT5	EXT PCT4	EXT PCT3	EXT PCT2	EXT PCT1	EXT PCT0
	Initial value	0	0	0	0	0	0	0	0

Note 1: The setting PCTL1BL2=0 should have been made in the register 0x39.
Note 2: The setting PCTL1BL2=1 should have been made in the register 0x39 (used in the page mode).

Table 5.3.8.3 Frame memory address (3/3)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x3D	R (Note 1)	MEMSTAT	—	—	—	—	—	—	EXT PCT8
	R (Note 2)	—	—	—	—	—	—	—	L1BF PCT8
	W	—	—	—	—	—	—	—	EXT PCT8
	Initial value	—	—	—	—	—	—	—	0

Note 1: The setting PCTL1BL2=0 should have been made in the register 0x39.
Note 2: The setting PCTL1BL2=1 should have been made in the register 0x39.

Write
Before reading from the receive port after the second horizontal error correction of the register 0x38, it is necessary to set the packet number and the byte number in the register. Specify the packet number of the starting byte and the starting byte number of the data to be read according to Table 5.3.6.1 "Data configuration of the receive frame memory after the second horizontal error correction".
Thereafter successive reads will be possible according to the "Access mode setting of the receive frame memory after the second horizontal error correction".

Read (PCTL1BL2=0)
It is possible to know the byte number and the packet number of the data to be read next by reading these registers 0x3B, 0x3C, and 0x3D.
However, it is necessary to set PCTL1BL2 of the register 0x39 to "0". Before reading these registers.

Read (PCTL1BL2=1)
The registers 0x3C and 0x3D indicate the frame memory address (packet number) of the data packet received after the first horizontal error correction, which is to be written next.

5.3.9 Reception status of the receive frame memory after the second horizontal error correction

Table 5.3.9 Frame synchronization status

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x37	R	BANK	—	—	—	BANK_ERCFR0	BANK_ERCFR1	BANK_ERCFR2	BANK_ERCFR3
	W	—	BANKLT_CLR	MOD_EXERC	EXPCTCNTSTARTB	BANK_ERCFR0	BANK_ERCFR1	BANK_ERCFR2	BANK_ERCFR3
	Initial value	—	0	0	0	0	0	0	0

Read

(1) DB0 to DB3: BANK_ERCFR3 to BANK_ERCFR0

When data is read after a receive interrupt after the second horizontal error correction, these four bits indicate whether the four packet groups listed in the following table are in a frame synchronization state or not.
The vertical error correction is carried out only when DB0=DB1=DB2=DB3=1. The second horizontal error correction is carried out only for the concerned packet group among DB0 to DB3. However, a separate setting and implementation of error correction for testing are required in the case of parity packets.

	Frame format		
	Format B	Format A1, A0	
DB3	Packet with a block number of 0 to 12.	A0, A1	Packet with a block number of 0 to 59
DB2	Packet with a block number of 13 to 135.	A0, A1	Packet with a block number of 60 to 129
DB1	Packet with a block number of 136 to 148.	A0, A1	Packet with a block number of 130 to 189
DB0	Packet with a block number of 149 to 271.	A0	Packet with a block number of 190 to 271
		A1	Packet with a block number of 190 to 283

Note: The packet numbers are expressed in this manual as 0 to 271 (A1: 0 to 283).

(2) DB7: BANK

For testing purposes only.

Write

This register is for making settings for testing and writing is prohibited under normal use.

5.4 TIMING INTERRUPT REGISTERS

There are the two timing interrupts of TIMINT_MAIN which operates in synchronization with the main channel and the timing interrupt TIMINT_SUB which operates in synchronization with the subchannel.
The block diagram of TIMINT_MAIN is shown in Figure 5.4.1.
The timing interrupt TIMINT_MAIN occurs when the packet number and byte number of the main channel match with the set interrupt timing.

The block diagram of TIMINT_SUB is shown in Figure 5.4.2.
The timing interrupt TIMINT_SUB occurs when the packet number, byte number, and frame number of the subchannel match with the set interrupt timing. It is possible to set TIMINT_SUB at intervals of 0 to 15 frames.
It is necessary to carry out initial setting of the timing of the packet number and frame number when synchronized with a subchannel.

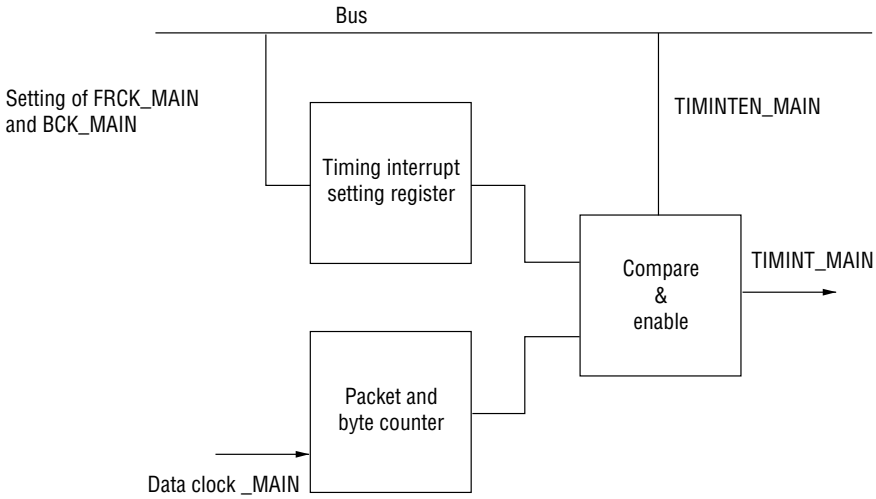


Figure 5.4.1 TIMINT_MAIN block diagram

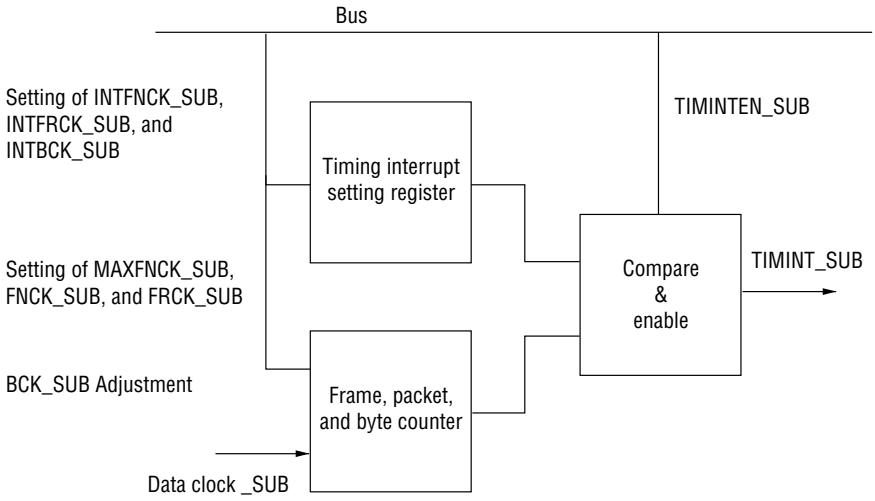


Figure 5.4.2 TIMINT_SUB block diagram

5.4.1 Timing interrupt mode

Since some of the interrupt timing registers have been mapped to the same address, this register controls their selection and timing enable conditions.

Table 5.4.1 Interrupt timing mode

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x05	W	—	TIMINTEN_SUB	SETCK1_SUB	SETCK0_SUB	RDBSCK_SUB	—	TIMINTEN_MAIN	SETINTCK_MAIN
	Initial value	—	0	0	0	0	—	0	0

(1) DB6: TIMINTEN_SUB

1: Activates the timing interrupt of the subchannel.
0: Disables the timing interrupt operation of the subchannel
Set the interrupt timing after making this bit "0" and change this bit to "1" after the setting is completed.

(2) DB5, DB4: SETCK1_SUB, SETCK0_SUB

DB5	DB4	Set mode	Description
1	1	SETMAX_SUB	Enables the setting of a count value of the maximum number of frames in the register 0x09.
1	0	SETINTCK_SUB	Enables the setting of the interrupt timing value in the registers 0x06 to 0x09.
0	1	SETTIMCK_SUB	Enables the setting of the initial value of the timer counter in the registers 0x08 to 0x09.
0	0	—	—

(3) DB3: RDBSCK_SUB

1: Makes it possible to read the block counter value of the subchannel.
0: Makes it possible to read the block counter value latched immediately before block synchronization of the subchannel.

(4) DB1: TIMINTEN_MAIN

1: Activates the timing interrupt of the main channel.
0: Disables the timing interrupt operation of the main channel.
Set the interrupt timing after setting this bit to "0", and set this bit to "1" after the interrupt timing setting is completed.

(5) DB0: SETINTCK_MAIN

1: Makes it possible to write the main channel interrupt timing values in the registers 0x16, 0x17, 0x1D, and 0x1E.
0: It is not possible to write the main channel interrupt timing values in the registers.

5.4.2 Interrupt byte number specification (main channel)

Table 5.4.2.1 Interrupt timing _MAIN (byte number 1/2)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x16	R	BCK7	BCK6	BCK5	BCK4	BCK3	BCK2	BCK1	BCK0
	W (Note 1)	INTBCK7	INTBCK6	INTBCK5	INTBCK4	INTBCK3	—	—	—
	Initial value	0	0	0	0	0	0	0	0

Note 1: The setting SETINTCK=1 should have been made in the register 0x05.

Table 5.4.2.2 Interrupt timing _MAIN (byte number 2/2)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x17	R	—	—	—	—	—	—	—	BCK8
	W (Note 1)	—	—	—	—	—	—	—	INTBCK8
	Initial value	—	—	—	—	—	—	—	0

Note 1: The setting SETINTCK=1 should have been made in the register 0x05.

Read
BCK8 (MSB) to BCK0 (LSB) indicate the bit numbers of the packet being received. The upper 6 bits indicate the byte number.

Write
This is the register for specifying the main channel interrupt byte number.
Before setting this register, set TIMINTEN_MAIN=1 and SETINTCK=1 in the register 0x05.
This matches with the received data byte number in a block synchronization state. The interrupt occurs at the leading part of a change in the byte number. Specify bytes 0 to 35 using the 6 bits INTBCK3 to INTBCK8.

5.4.3 Interrupt packet number specification (main channel)

Table 5.4.3.1 Interrupt timing _MAIN (packet number 1/2)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x1D	R	FRCK7	FRCK6	FRCK5	FRCK4	FRCK3	FRCK2	FRCK1	FRCK0
	W (Note 1)	INT FRCK7	INT FRCK6	INT FRCK5	INT FRCK4	INT FRCK3	INT FRCK2	INT FRCK1	INT FRCK0
	Initial value	0	0	0	0	0	0	0	0

Note 1: The setting SETINTCK=1 should have been made in the register 0x05.

Table 5.4.3.2 Interrupt timing _MAIN (packet number 2/2)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x1E	R	ACTMC0 _SUB	ACTMC2	ACTMC1	ACTMC0	—	—	—	FRCK8
	W (Note 1)	—	—	—	—	—	—	INT ALLFRCKTIM	INT FRCK8
	Initial value	0	0	0	0	—	—	0	0

Note 1: The setting SETINTCK=1 should have been made in the register 0x05.

Read
FRCK8 (MSB) to FRCK0 (LSB) indicate the packet number of the packet being received.

Write
This is the register for specifying the main channel interrupt packet number.
Timing interrupts occur at all packets when the setting ALLFRCKTIM=1 is made.
Before setting this register, set TIMINTEN_MAIN=0 and SETINTCK=1 in the register 0x05.
This matches with the packet number of received data in a frame synchronization state.

5.4.4 Interrupt byte number specification (subchannel)

Table 5.4.4.1 Interrupt timing _SUB (byte number 1/2)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x06	R (Note 1)	PRE_BCK7 _SUB	PRE_BCK6 _SUB	PRE_BCK5 _SUB	PRE_BCK4 _SUB	PRE_BCK3 _SUB	PRE_BCK2 _SUB	PRE_BCK1 _SUB	PRE_BCK0 _SUB
	R (Note 2)	BCK7 _SUB	BCK6 _SUB	BCK5 _SUB	BCK4 _SUB	BCK3 _SUB	BCK2 _SUB	BCK1 _SUB	BCK0 _SUB
	W (Note 3)	INTBCK7 _SUB	INTBCK6 _SUB	INTBCK5 _SUB	INTBCK4 _SUB	INTBCK3 _SUB	—	—	—
	Initial value	0	0	0	0	0	0	0	0

Note 1: The setting RDBSCK_SUB=0 (R_05[DB3]=0) should have been made in the register 0x05.
Note 2: The setting RDBSCK_SUB=1 (R_05[DB3]=1) should have been made in the register 0x05.
Note 3: The setting SETINTCK_SUB (R_05[DB4]=0, R_05[DB5]=1) should have been made in the register 0x05.

Table 5.4.4.2 Interrupt timing _SUB (byte number 2/2)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x07	R (Note 1)	—	—	—	—	—	—	—	PRE_BCK8 _SUB
	R (Note 2)	—	—	—	—	—	—	—	BCK8 _SUB
	W (Note 3)	—	—	—	—	—	—	—	INTBCK8 _SUB
	Initial value	—	—	—	—	—	—	—	0

Note 1: The setting RDBSCK_SUB=0 (R_05[DB3]=0) should have been made in the register 0x05.
Note 2: The setting RDBSCK_SUB=1 (R_05[DB3]=1) should have been made in the register 0x05.
Note 3: The setting SETINTCK_SUB (R_05[DB4]=0, R_05[DB5]=1) should have been made in the register 0x05.

Read (RDBSCK=1)
BCK8_SUB (MSB) to BCK0_SUB (LSB) indicate the bit numbers of the packet being received. The upper 5 bits indicate the byte number.

Read (RDBSCK=0)
PRE_BCK8_SUB (MSB) to PRE_BCK0_SUB (LSB) indicate the bit numbers of the packet immediately before the subchannel enters block synchronization.

Write (SETINTCK_SUB)
This is the register for specifying the subchannel interrupt byte number.
Before setting this register, make the setting of SETINTCK_SUB in the register 0x05.
This matches with the byte number of received data in a block synchronization state. The interrupt occurs at the leading part of a change in the byte number.
Specify bytes 0 to 35 using the 6 bits INTBCK3 to INTBCK8.

5.4.5 Interrupt packet number setting (subchannel)

Table 5.4.5 Interrupt timing setting _SUB (packet number)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x08	R	FRCK7 _SUB	FRCK6 _SUB	FRCK5 _SUB	FRCK4 _SUB	FRCK3 _SUB	FRCK2 _SUB	FRCK1 _SUB	FRCK0 _SUB
	W (Note 1)	FRCK7 _SUB	FRCK6 _SUB	FRCK5 _SUB	FRCK4 _SUB	FRCK3 _SUB	FRCK2 _SUB	FRCK1 _SUB	FRCK0 _SUB
	W (Note 2)	INT FRCK7 _SUB	INT FRCK6 _SUB	INT FRCK5 _SUB	INT FRCK4 _SUB	INT FRCK3 _SUB	INT FRCK2 _SUB	INT FRCK1 _SUB	INT FRCK0 _SUB
	Initial value	0	0	0	0	0	0	0	0

Note 1: The setting SETTIMCK_SUB (R_05[DB4]=1, R_05[DB5]=0) should have been made in the register 0x05.
Note 2: The setting SETINTCK_SUB (R_05[DB4]=0, R_05[DB5]=1) should have been made in the register 0x05.

Read
FRCK8_SUB (MSB) to FRCK0_SUB (LSB) indicate the packet number of the packet being received. (FRCK8_SUB is allocated to DB0 of the register 0x09.)

Write (FRCK8_SUB to FRCK0_SUB)
This is the register for specifying the initial value of the packet number in the subchannel packet counter.
Since the subchannel does not have a built-in frame synchronization circuit, it is necessary for the user to set the packet number. To obtain the packet number, achieve frame synchronization temporarily with the main channel, and write that packet number. (FRCK8_SUB is allocated to DB0 of the register 0x09.)

Write (INTFRCK0_SUB to INTFRCK8_SUB)
This is the register for specifying the interrupt packet number of the subchannel.
Timing interrupts occur at all packets if the setting INTALLFRCK_SUB=1 (register 0x09) is made.
Carry out the setting of SETINTCK_SUB in the register 0x09 before setting this register.
(INTFRCK8_SUB is allocated to DB0 of the register 0x09.)

5.4.6 Interrupt frame number setting (subchannel)

Table 5.4.6 Interrupt timing setting _SUB (frame interval)

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x09	R	—	—	—	FNCK3 _SUB	FNCK2 _SUB	FNCK1 _SUB	FNCK0 _SUB	FNCK8 _SUB
	W (Note 1)	—	—	—	FNCK3 _SUB	FNCK2 _SUB	FNCK1 _SUB	FNCK0 _SUB	FNCK8 _SUB
	W (Note 2)	—	—	INT ALLFRCK _SUB	INT FNCK3 _SUB	INT FNCK2 _SUB	INT FNCK1 _SUB	INT FNCK0 _SUB	INT FNCK8 _SUB
	W (Note 3)	—	—	—	MAX FNCK3 _SUB	MAX FNCK2 _SUB	MAX FNCK1 _SUB	MAX FNCK0 _SUB	—
	Initial value	—	—	0	0	0	0	0	0

Note 1: The setting SETTIMCK_SUB (R_05[DB4]=1, R_05[DB5]=0) should have been made in the register 0x05.
Note 2: The setting SETINTCK_SUB (R_05[DB4]=0, R_05[DB5]=1) should have been made in the register 0x05.
Note 3: The setting SETMAX_SUB (R_05[DB4]=1, R_05[DB5]=0) should have been made in the register 0x05.

Read (FNCK0 to FNCK3)
FNCK3 (MSB) to FNCK0 (LSB) indicate the frame number being counted.

Write (FRCK0_SUB to FRCK3_SUB)
This is the register for specifying the initial value of the frame number in the 4-bit frame number counter of the subchannel.
The 4-bit frame number counter is one for generating subchannel timing interrupts at intervals of 0 to 15 frames.
The frame interval is specified by MAXFNCK0_SUB to MAXFNCK3_SUB.

Write (INTFNCK0_SUB to INTFNCK3_SUB)
This is the register for specifying the subchannel interrupt frame number. The range of setting is 0 to 15. Carry out the settings of TIMINTEN_SUB and SETINTCK of the register 0x05 before setting this register.

Write (MAXFNCK0_SUB to MAXFNCK3_SUB)
This is the register for setting the maximum value of the frame number counter. The range of setting is 0 to 15.
When the frame number counter reaches the set value, it is reset to "0" and continues counting.

5.4.7 Clock timing adjustment (subchannel)

Table 5.4.7 Subchannel BCK adjustment

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x0A	W	—	—	—	—	BCKINC_SUB	B2	B1	B0
	Initial value	—	—	—	—	0	0	0	0

The subchannel packet interval is adjusted in units of a bit.
When intermittent reception is being made at intervals of several frames, this function enables the accurate setting of the position of the packet to be received next. The range of adjustment at a time is ±7 bits. Carry out this adjustment at the most once per packet when no reception is being made. The number of bits of adjustment required is the difference between "16" and the value of the registers 0x06 to 0x07 when a subchannel packet is received.

(1) DB3: BCKINC_SUB

1: Added the number of correction bits set in DB0 to DB2.
0: Eliminated the number of correction bits set in DB0 to DB2.

(2) DB0 to DB2: B0 to B2

These specify the range of adjustment (in number of bits). The maximum value is 7 bits.

DB2	DB1	DB0	Correction bit
0	0	0	No correction
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

5.5 CLOCK REGENERATION REGISTERS

5.5.1 Fixed phase adjustment

Table 5.5.1 Fixed phase adjustment

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x0B	W	—	B6	B5	B4	B3	B2	B1	B0
	Initial value	—	0	0	0	0	0	0	0

The phase of the regenerated data clock is adjusted. Use with the initial value left unchanged.

5.5.2 Integration constant before synchronization

Table 5.5.2 Integration constant before synchronization

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x0C	W	—	—	—	—	B3	B2	B1	B0
	Initial value	—	—	—	—	0	0	1	0

This register specifies the number of times of extracting the timing necessary for carrying out phase control before block synchronization.
Specify "6" (0x06) as a typical setting value.

5.5.3 Integration constant after synchronization

Table 5.5.3 Integration constant after synchronization

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x0D	W	—	—	B5	B4	B3	B2	B1	B0
	Initial value	—	—	0	1	1	0	0	0

This register specifies the number of times of extracting the timing necessary for carrying out phase control after block synchronization.
Specify "16" (0x10) as a typical setting value.

5.5.4 Phase correction step

Table 5.5.4 Phase correction step

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x0E	W	—	B6	B5	B4	—	B2	B1	B0
	Initial value	—	0	0	1	—	0	0	1

This register is used for setting the phase correction step width of the digital PLL for data clock regeneration.
DB0 to DB2: The phase correction step before block synchronization.
DB4 to DB6: The phase correction step after block synchronization.

DB2 (DB6)	DB1 (DB5)	DB0 (DB4)	Phase correction step width
0	0	0	Prohibited
0	0	1	250nSec
0	1	0	500nSec
0	1	1	750nSec
1	0	0	1000nSec
1	0	1	1250nSec
1	1	0	1500nSec
1	1	1	1750nSec

Set "1000ns" (0x33) as a typical setting value.

5.6 BLOCK SYNCHRONIZATION REGISTERS

5.6.1 Allowable number of BIC errors

Table 5.6.1 Allowable number of BIC errors

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x10	W	BICGATE SEL1_SUB	BICGATE SEL0_SUB	—	—	B3	B2	B1	B0
	Initial value	0	1	—	—	0	1	1	0

This is a specification related to the synchronization and clock regeneration processing of the MSM9563, and consists of the specification of the allowable number of error bits in the block identification code (BIC).

(1) DB1 to DB0: Allowable number of BIC errors before block synchronization (common to main channel and subchannels)

Set value		Allowable number of BIC errors before block synchronization
DB1	DB0	
0	0	0
0	1	1
1	0	2
1	1	3

(2) DB3 to DB2: Allowable number of BIC errors after block synchronization (common to main channel and subchannels)

Set value		Allowable number of BIC errors after block synchronization
DB3	DB2	
0	0	0
0	1	1
1	0	2
1	1	3

(3) DB7 to DB6: BICGATESEL1_SUB to BICGATE SEL0_SUB

The segments given in the following table are added to the BIC detection segments in addition to the leading two bytes of the packet when used in the subchannel mode.

Set value		BIC Detection gate width
DB7	DB6	
0	0	—
0	1	±1 Byte
1	0	±1.5 Byte
1	1	±2 Byte

5.6.2 Number of block synchronization backward protection steps

Table 5.6.2 Number of block synchronization backward protection steps

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x11	W	—	—	B1_SUB	B0_SUB	—	—	B1	B0
	Initial value	—	—	0	0	—	—	0	1

This register is used for setting the number of successive detections of the block identification code (BIC) before considering that a block has been synchronized.

Number of main channel block synchronization backward protection steps

Set value		Number of block synchronization backward protection steps	Number of successive detections of BIC
DB1	DB0		
0	0	1	1
0	1	2	2
1	0	3	3
1	1	4	4

Number of subchannel block synchronization backward protection steps

Set value		Number of block synchronization backward protection steps	Number of successive detections of BIC
DB5	DB4		
0	0	1	1
0	1	2	2
1	0	3	3
1	1	4	4

5.6.3 Number of block synchronization forward protection steps

Table 5.6.3 Number of block synchronization forward protection steps

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x12	R/W	B3_SUB	B2_SUB	B1_SUB	B0_SUB	B3	B2	B1	B0
	Initial value	1	0	0	0	1	0	0	0

Write

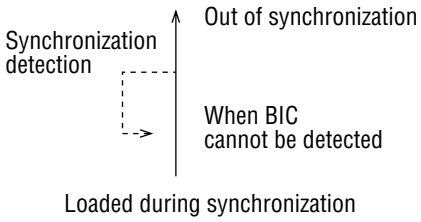
This register is used for setting the number of successive detection failures of the block identification code (BIC) before considering that the block has been synchronized.
DB0 to DB3: Setting of the main channel block synchronization forward protection steps
DB4 to DB7: Setting of the subchannel block synchronization forward protection steps

DB3 (DB7)	DB2 (DB6)	DB1 (DB5)	DB0 (DB4)	Number of block synchronization forward protection steps
0	0	0	0	0 (Prohibited)
0	0	0	1	1
↓	↓	↓	↓	↓
1	1	1	1	15

Read

When BICs cannot be detected successively in a block synchronization state, the number of detection failures is decremented from the number of block synchronization forward protection steps, and when the value of this register changes from 1 to 0, the block is considered to have been out of synchronization.

DB3 (DB7)	DB2 (DB6)	DB1 (DB5)	DB0 (DB4)	Remaining number of block synchronization forward protection steps
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
1	1	1	1	15



5.6.4 Block synchronization monitor

Table 5.6.4 Block synchronization monitor

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x13	R	—	—	—	BSYNC_SUB	—	—	—	BSYNC
	Initial value	—	—	—	0	—	—	—	0

DB0: Main channel block synchronization state
- 0: Block out-of-synchronization
- 1: Block synchronized

DB4: Subchannel block synchronization state
- 0: Block out-of-synchronization
- 1: Block synchronized

5.6.5 Setting/clearing block synchronization

Table 5.6.5 Setting/clearing block synchronization

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x14	W	—	—	B1_SUB	B0_SUB	—	—	B1	B0
	Initial value	—	—	0	0	—	—	0	0

Setting/clearing main channel block synchronization

DB1	DB0	Setting or clearing synchronization
1	0	Clearing synchronization
0	1	Setting synchronization

Setting/clearing subchannel block synchronization

DB5	DB4	Setting or clearing synchronization
1	0	Clearing synchronization
0	1	Setting synchronization

5.7 FRAME SYNCHRONIZATION REGISTERS

5.7.1 Number of frame synchronization backward protection steps

Table 5.7.1 Number of frame synchronization backward protection steps

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x18	W	—	—	—	—	—	—	B1	B0
	Initial value	—	—	—	—	—	—	0	1

This register is used for setting the number of successive detections of synchronization points required before considering that the frame has been synchronized.

DB1	DB0	Number of frame synchronization backward protection steps
0	0	1
0	1	2
1	0	3
1	1	4

5.7.2 Number of frame synchronization forward protection steps

Table 5.7.2 Number of frame synchronization forward protection steps

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x19	R/W	—	—	—	—	B3	B2	B1	B0
	Initial value	—	—	—	—	0	1	0	0

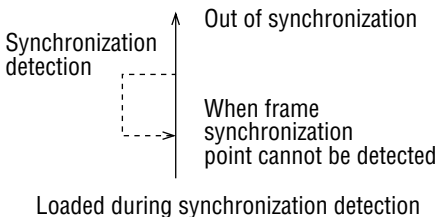
Write

This register is used for setting the number of successive detection failures of synchronization points before considering that the frame has been out-of-synchronized.

DB3	DB2	DB1	DB0	Number of frame synchronization forward protection steps
0	0	0	0	0 (Prohibited)
0	0	0	1	1
↓	↓	↓	↓	↓
1	1	1	1	15

Read
When synchronization points cannot be detected successively in a frame synchronization state, the number of detection failures is decremented from the set number of frame synchronization forward protection steps, and when the value of this register changes from 1 to 0, the frame is considered to have been out-of-synchronization.

DB3	DB2	DB1	DB0	Remaining number of frame synchronization forward protection steps
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
1	1	1	1	15



5.7.3 Frame synchronization monitor

Table 5.7.3 Frame synchronization monitor

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x1A	R	—	—	—	—	—	—	—	FSYNC
	Initial value	—	—	—	—	—	—	—	0

DB0: Frame synchronization monitor
0: Frame out-of-synchronization
1: Frame synchronized

5.7.4 Setting frame synchronization

Table 5.7.4 Setting frame synchronization

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x1B	W	×	×	×	×	×	×	×	×
	Initial value	×	×	×	×	×	×	×	×

5.7.5 Clearing frame synchronization

Table 5.7.5 Clearing frame synchronization

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x1C	W	×	×	×	×	×	×	×	×
	Initial value	×	×	×	×	×	×	×	×

5.8 ERROR CORRECTION REGISTERS

The first horizontal error correction, vertical error correction, and the second horizontal error correction have been automated.
The results of correction and CRC can be read together with the receive data from the receive port after the first horizontal error correction and the receive port after the second horizontal error correction.
In addition, the number of corrections and the threshold value have been set optimally.
Therefore, normally, there is no need to set the registers 0x20, 0x21, 0x22, 0x23, 0x24, and 0x25.

5.8.1 Clearing address

Table 5.8.1 Clearing address

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x20	W	—	—	—	—	—	—	B1	B0
	Initial value	—	—	—	—	—	—	0	0

	B1	B0
Address Clear	0	1
ERC0_CHG (for testing)	1	0

5.8.2 Error correction data port

Table 5.8.2 Error correction data port

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x21	R	B7	B6	B5	B4	B3	B2	B1	B0
	W	B7	B6	B5	B4	B3	B2	B1	B0
	Initial value	—	—	—	—	—	—	—	—

5.8.3 Error correction start

Table 5.8.3 Error correction start

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x22	R	—	—	—	—	—	Second horizontal correction state	Vertical correction state	First horizontal correction state
	W	—	—	—	—	—	Start second horizontal correction	Start vertical correction	Start first horizontal correction
	Initial value	—	—	—	—	—	—	—	—

5.8.4 Number of corrections and error correction results

Table 5.8.4 Number of corrections and error correction results

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x23	R	Result of second horizontal correction	Result of first horizontal correction	—	—	—	—	Second horizontal CRC result	First horizontal CRC result
	W	Number of second horizontal corrections _B2	Number of second horizontal corrections _B1	Number of second horizontal corrections _B0	Number of vertical corrections _B2	Number of vertical corrections _B1	Number of vertical corrections _B0	MOD_ VSTAT RAM	MOD_ ERC0 CHG
	Initial value	1	1	1	1	1	0	1	1

5.8.5 Results of vertical error correction

Table 5.8.5 Results of vertical error correction

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x24	R	CRCOUT7	CRCOUT6	CRCOUT5	CRCOUT4	CRCOUT3	CRCOUT2	CRCOUT1	CRCOUT0
	Initial value	0	0	0	0	0	0	0	0

5.8.6 Number of corrections and threshold value

Table 5.8.6 Number of corrections and threshold value

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x25	W	Number of first horizontal corrections _B2	Number of first horizontal corrections _B1	Number of first horizontal corrections _B0	Threshold value TH4	Threshold value TH3	Threshold value TH2	Threshold value TH1	Threshold value TH0
	Initial value	1	1	1	0	1	1	1	0

5.9 LAYER 4 CRC REGISTERS

5.9.1 Layer 4 CRC registers

Table 5.9.1 Layer 4 CRC register

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x28	R	L4CRC OUT	—	—	—	—	—	—	—
	W	MOD2	MOD1	MOD0	—	—	—	MEMTST	CLRCRC
	Initial value	1	1	0	—	0	0	0	0

Write

(1) DB0: CLRCRC
Write a "1" before executing layer 4 CRC
However, (111X0001) is valid only when DB5=DB6=DB7=1.

(2) DB1: MEMTEST
The use of any value other than "0" is prohibited.

(3) DB5 to DB7: Setting of the test mode
Use one of the modes given in the following table.

Set mode	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CLRCRC	1	1	1	—	0	0	0	1
Other than CLRCRC	0	1	0	—	—	—	0	—
	0	0	1	—				
	0	0	0	—				

Read

(1) DB7: L4CRCOUT (Display of layer 4 CRC result)
1: There is an error in the layer 4 CRC result.
0: The layer 4 CRC result is normal.

5.9.2 Layer 4 CRC data port

Table 5.9.2 Layer 4 CRC data port

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x29	R	B7	B6	B5	B4	B3	B2	B1	B0
	W	B7	B6	B5	B4	B3	B2	B1	B0
	Initial value	×	×	×	×	×	×	×	×

Write the data group for which CRC processing is to be made in units of a byte at a cycle period of 620ns or more.

5.9.3 Layer 4 CRC result

Table 5.9.3 Layer 4 CRC result

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x2A	R	—	—	—	—	—	—	—	L4CRC result
	Initial value	—	—	—	—	—	—	—	0

(1) DB0: L4CRC result
0: Normal
1: Error
Read out the layer 4 CRC result when a time of 1.2µs or more has elapsed after writing the last data of the data group.

5.9.4 Layer 4 CRC register

This is the register for writing the initial value directly in the CRC computation registers and for reading out the intermediate result.
It is possible to execute the layer 4 CRC processing of a short data group by interrupting the layer 4 CRC processing of a long data group.

Table 5.9.4.1 Layer 4 CRC register upper 8 bits

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x2B	R/W	B7	B6	B5	B4	B3	B2	B1	B0
	Initial value	0	0	0	0	0	0	0	0

Table 5.9.4.2 Layer 4 CRC register lower 8 bits

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x2C	R/W	B7	B6	B5	B4	B3	B2	B1	B0
	Initial value	0	0	0	0	0	0	0	0

5.10 ANALOG TEST REGISTER

Table 5.10.1 Analog test

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x30	W	—	DETO DTST	M2	M1	M0	SGAIN1	SGAIN0	DETC
	Initial value	—	0	0	0	0	0	0	0

(1) DB0: DETC
For testing purposes only.
Use normally with DETC=0.

(2) DB2 to DB1: SGAIN1 to SGAIN0
These set the variable gain amplifier for the analog signal input (composite signal).
Set so that peak value of the analog input signal (composite signal)×gain=0.5 to 0.9$V_{P\text{-}P}$.

DB2 (SGAIN1)	DB1 (SGAIN0)	Gain
0	0	× 1
0	1	× 1.5
1	0	× 2
1	1	× 3

(3) DB3 to DB5: M2 to M0
This register controls the monitor terminal (MON pin) for the analog section output waveform.

DB5 (M2)	DB4 (M1)	DB3 (M0)	MON Pin (pin1)
0	0	0	Internal monitor pin power-off, Hz output
0	0	1	LPF output of input stage
0	1	0	BPF output 2
0	1	1	BPF output 4
1	0	0	BPF output 6
1	0	1	BPF output 8
1	1	0	Internal amplifier output
1	1	1	Equivalent waveform output (for observing the eye pattern)

(4) DB6: DEST0DTST
For testing purpose only.
Normally use with the setting DB6=0.

DB6 (DETODTST)	DB0 (DETC)	DET (data identification circuit) input control
0	0	AIN pin input enable (FM multiplex broadcast reception)
0	1	ADETIN pin input enable (analog input)
1	0	ADETIN pin input enable (digital input)
1	1	

5.11 POWER DOWN REGISTER

Table 5.11 Power down

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x31	W	—	XCK2	XCK1	XCK0	—	B2	B1	B0
	Initial value	—	0	0	0	—	0	0	0

(1) DB4 to DB6: XCK0 to XCK2 (setting the divided frequency of external clock)
Set the divided frequency of the clock that is output to the XOUT pin, as follows (when $\overline{\text{XOUTC}}$=0)

DB6	DB5	DB4	XOUT Pin output clock frequency
0	0	0	8.192 MHz
0	0	1	4.096 MHz
0	1	0	2.048 MHz
0	1	1	1.024 MHz
1	0	0	0.512 MHz
1	0	1	0.256 MHz
1	1	0	0.128 MHz
1	1	1	0.064 MHz

(2) DB2: External clock input
This controls the operation of the crystal oscillator circuit as follows when the $\overline{\text{XOUTC}}$ pin is "1". Also, in this case, the XOUT output pin is set to the "L" level.
0: The operation of the crystal oscillator circuit is stopped.
1: The crystal oscillator circuit is acrivated.

When the $\overline{\text{XOUTC}}$ pin is "0", the crystal oscillator circuit will be operating continuously and the XOUT pin also will be outputting the clock signal continuously.

(3) DB1: Digital section power down
0: The power is down and the internal clock stops at the "H" level.
1: The power is turned on and the clock for operating the digital section starts from the "H" level.

(4) DB0: Analog section power down
0: Power down (operation stops)
1: Power on (several milliseconds will be required for the circuit operation to become stable after the power is turned on.)

5.12 TEST CONTROL REGISTERS

5.12.1 Test control 0

Table 5.12.1 Test control 0

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x32	W	B7	B6	B5	—	—	—	—	—
	Initial value	0	0	0	—	—	—	—	—

This is the register for controlling the selection of the test output pins (MOUT0 to MOUT4), and is used for testing only.

Pin name	Set value					
	Extention port	LSI internal signal monitor				
	0xC0, 0xA0, 0x00	0x20 (TST0)	0x40 (TSTT1)	0x60 (TSTB0)	0x80 (TSTB1)	0xE0 (TSTC)
MOUT0	DB0 of register 0x0F	BPF-LimOut	TS11	FRCK0	FSYNC (Note 1)	
MOUT1	DB1 of register 0x0F	Delay detector Out	TS21	FRCK1	BSYNC (Note 2)	
MOUT2	DB2 of register 0x0F	LPF-LimOut	TS10	FRCK2	RAMOUT	BIC0 (Note 3)
MOUT3	DB3 of register 0x0F	SCF clock	GATE	FRCK3	BICDET2	BIC1 (Note 3)
MOUT4	DB4 of register 0x0F	Fixed to "L"	PHCK1	BCK	BICDET	BICDET1 (Note 3)

Note 1: FSYNC
1: Frame synchronized
0: Frame out-of-synchronization

Note 2: BSYNC
1: Block synchronized
0: Block out-of-synchronization

Note 3: BIC Detection

BICDET1	BIC1	BIC0	BIC NO.
1	0	0	1
1	0	1	2
1	1	0	3
1	1	1	4
0	—	—	Not detected

5.12.2 Test control 1

Table 5.12.2 Test Control 1

Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x33	W	—	Delay detector output control 1	Delay detector output control 0	Serial output control 1	PN Decoding control	Differential decoding control	Clock output control	Serial output control 0
	Initial value	—	0	0	0	0	1	0	0

This register controls serial receive data and the switching of the test output pins (MOUT5 and MOUT6). This is used for testing only.

(1) DB0, DB4: Serial receive data output

DB4	DB0	MOUT6 pin output
0	0	Fixed to "L"
0	1	Serial receive data after descrambling
1	0	Serial receive data before descrambling
1	1	

(2) DB1: 16kHz regeneration data clock
0: The MOUT5 pin is fixed to "L".
1: A 16kHz regeneration data clock is output to the MOUT5 pin.

(3) DB2: Differential decoding control
0: Performs differential decoding to input data.
1: Does not perform differential decoding.
(This is used for receiving FM multiplex broadcast)

(4) DB3: Descramber control
0: Descrambles data other than BIC.
(This is used for receiving FM multiplex broadcast.)
1: Does not descramble other than BIC.

(5) DB5, DB6: Delay detector output control

DB6	DB5	Delay detector control
0	0	ENOR (FM multiplex broadcast reception)
0	1	Through (data before 1T)
1	0	EOR
1	1	

5.13 EXTENSION PORT REGISTER

It is possible to output the write data (DB0 to DB4) of this register to the monitor output terminal by setting 0xC0, and 0xA0, or 0x00 in the register 0x32.

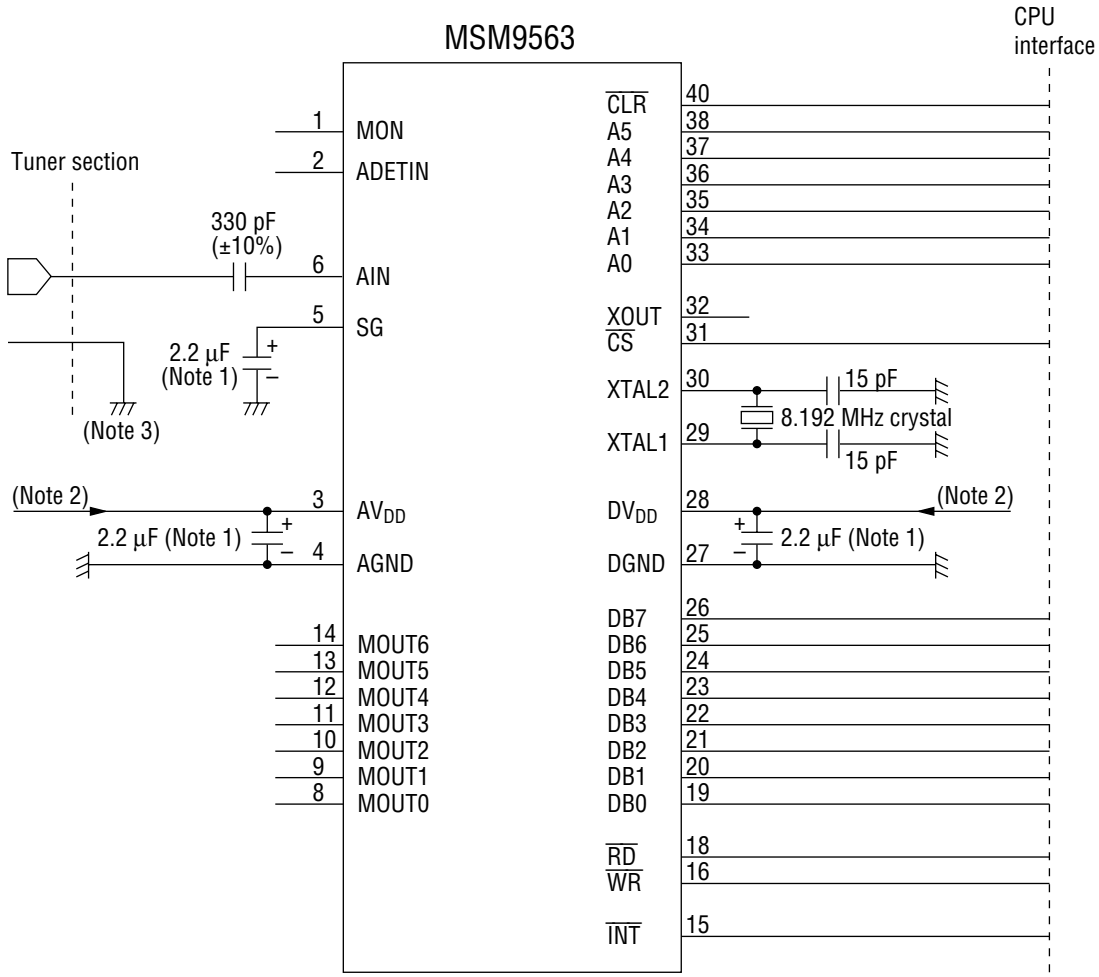
Table 5.13 Extension port register

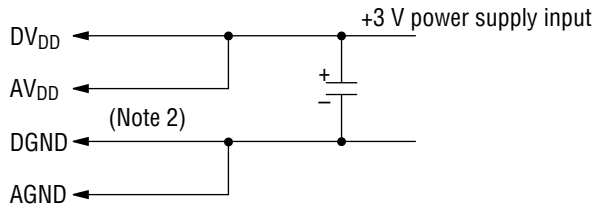
Address	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x0F	W	—	—	—	DB4	DB3	DB2	DB1	DB0
	Initial value	—	—	—	0	0	0	0	0

Chapter 6

EXTERNAL CONNECTION EXAMPLE

6. EXTERNAL CONNECTION EXAMPLE



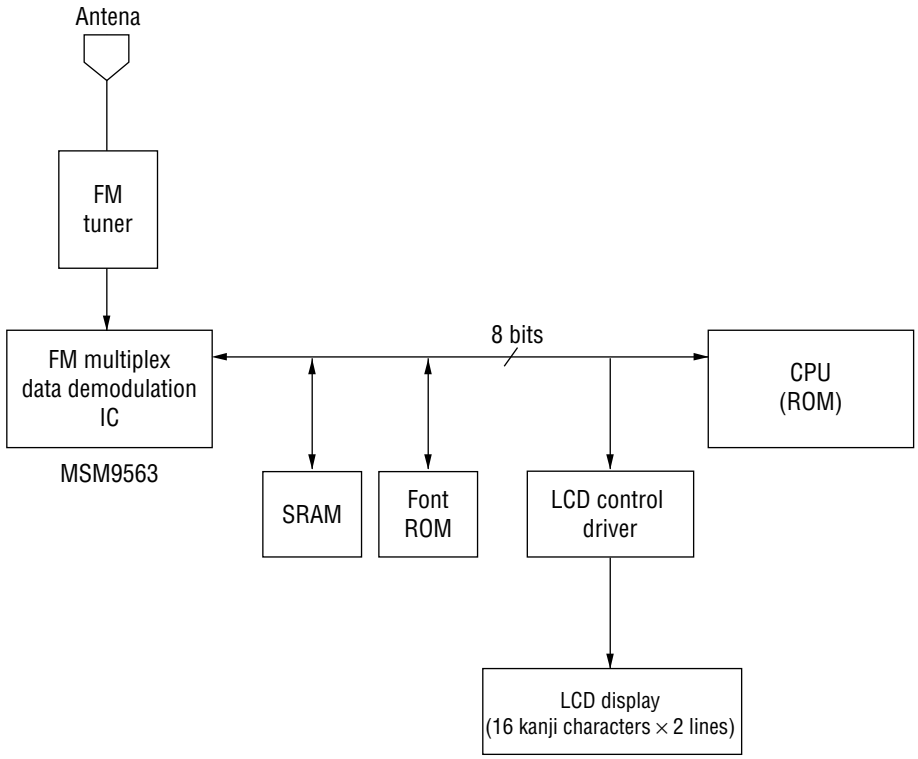


(Note 1) Use a tantalum capacitor.
(Note 2) The AV_{DD} and DV_{DD} should have different paths, respectively.
(Note 3) The AGND and tuner ground should use the same ground.

Chapter 7

APPLICATION CIRCUIT

7. APPLICATION CIRCUIT



APPENDIX

LIST OF REGISTERS (1/2)

	MSM9552/9553 (reference)					MSM9562/9563						
Register address	Category	Register name	Initial value	Recommended value *1	R/W	Category	Register name	Page No.	Initial value	Recommended value *2	R/W	Register address
0x00	Interrupt	Interrupt cause	0-000000	—	R/W	Interrupt	Interrupt register	5-5	0000-000	—	R/W	0x00
0x01		Interrupt mask	--000000	—	W		Interrupt mask	5-6	0000-00-	—	W	0x01
0x02	Receive data	Receive block condition	00000000	—	R	Receive data	Receive port selection after first horizontal error correction	5-7	-------0	—	W	0x02
0x03		Receive data and first horizontal error correction data port	Undefined	—	R		Receive port after first horizontal error correction	5-8	Undefined	—	R/W	0x03
0x04		Receive RAM, data accumulation condition, and address clear	------0-	11111111	W	Operating mode	Main channel/subchannel mode setting	5-1	---0---1	—	W	0x04
0x05						Timing interrupt	Timing interrupt mode	5-22	-0000-00	—	W	0x05
0x06							Interrupt timing _SUB (byte number 1/2)	5-24	00000000	—	R/W	0x06
0x07		BIC Monitor	----000	—	R		Interrupt timing _SUB (byte number 2/2)	5-25	-------0	—	R/W	0x07
0x08	Clock regeneration	Fixed phase adjustment	-0000000	10000000	R		Interrupt timing _SUB (packet number)	5-25	00000000	—	R/W	0x08
0x09		Bit gate	----0000	11110000	R		Interrupt timing _SUB (frame interval)	5-26	--000000	—	R/W	0x09
0x0A		Integration constant (1/4)	----0010	11110110	R		Clock timing adjustment (subchannel)	5-27	----0000	—	W	0x0A
0x0B		Integration constant (2/4)	----0010	11110110	R	Clock regeneration	Fixed phase adjustment	5-28	-0000000	—	W	0x0B
0x0C		Integration constant (3/4)	--011000	11010000	R		Integration constant before sysnchronization	5-28	----0010	----0110	W	0x0C
0x0D		Integration constant (4/4)	--011000	11010000	R		Integration constant after synchronization	5-28	--011000	--010000	W	0x0D
0x0E		Phase correction step	----0101	11111111	R		Phase correction step	5-29	-001-001	-011-011	W	0x0E
0x10	Block synchronizaiton	Allowable number of BIC errors	----0110	11111001	W	Block synchronization	Allowable number of BIC errors	5-30	01--0110	00--1001	W	0x10
0x11		Number of block synchronization backward protection steps	------01	11111101	W		Number of block synchronization backward protection steps	5-31	--00--01	--01--10	W	0x11
0x12		Number of block synchronization forward protection steps	----1000	11111111	W		Number of clock synchronization forward protection steps	5-32	10001000	01001111	R/W	0x12
0x13		Block synchronization monitor	0000---0	—	R		Block synchronization monitor	5-33	---0---0	—	R	0x13
0x14							Block synchronization setting/clearing	5-33	--00--00	—	W	0x14
0x15		Block synchronization clearing	xxxxxxxx	—	W							0x15
0x16		In-block bit number monitor (1/2)	00000000	—	R	Timing interrupt	Interrupt timing _MAIN (byte number 1/2)	5-23	00000000	—	R/W	0x16
0x17		In-block bit number monitor (2/2)	-------0	—	R		Interrupt timing _MAIN (byte number 2/2)	5-23	-------0	—	R/W	0x17
0x18	Frame synchronization	Number of block synchronization backward protection steps	------01	11111100	W	Frame synchronization	Number of frame synchronization backward protection steps	5-34	------01	------00	W	0x18
0x19		Number of block synchronization forward protection steps	----0100	11110100	W		Number of frame synchronization forward protection steps	5-34	----0100	—	R/W	0x19
0x1A		Frame synchronization monitor	0000--0-	—	R		Frame synchronization monitor	5-35	-------0	—	R	0x1A
0x1B							Frame synchronization setting	5-35	Undefined	—	W	0x1B
0x1C		Frame synchronization clearing	xxxxxxxx	—	W		Frame synchronization clearing	5-35	Undefined	—	W	0x1C
0x1D		In-frame block number monitor (1/2)	00000000	—	R	Timing interrupt	Interrupt timing _MAIN (packet number 1/2)	5-23	00000000	—	R/W	0x1D
0x1E		In-frame block number monitor (2/2)	-------0	—	R		Interrupt timing _MAIN (packet number 2/2)	5-24	0000--00	—	R/W	0x1E
0x1F		International frame format specification	------10	—	W	Operating mode	Frame format specification	5-1	------10	—	W	0x1F

*1 Unused bits are entered as "1".

*2 Unused bits are entered as "—".

LIST OF REGISTERS (2/2)

	MSM9552/9553 (reference)					MSM9562/9563						
Register address	Category	Register name	Initial value	Recommended value	R/W	Category	Register name	Page No.	Initial value	Recommended value	R/W	Register address
0x20	Error correction	Internal address counter clear	xxxxxxxx	—	W	Error correction	Internal address counter clear	5-36	------00	—	W	0x20
0x21		Data transfer port for error correction	Undefined	—	R/W		Data transfer port for error correction	5-36	--------	—	R/W	0x21
0x22		Start signal for error correction	-----000	—	R/W		Start signal for error correction	5-36	--------	—	R/W	0x22
0x23		CRC Result display/second horizontal error	-----0-0	—	R		Number of corrections and error correction result	5-37	11111011	—	R/W	0x23
0x24		Error correction result display	00000000	—	R		Vertical error correction result	5-37	00000000	—	R	0x24
0x25		Majority logic threshold value	---01000	11101001	W		Number of vertical error corrections and threshold value	5-37	11101110	—	W	0x25
0x28	Layer 4 CRC	Clear layer 4 CRC registers	11000000		R/W	Layer 4 CRC	Layer 4 CRC	5-38	110-0000	—	R/W	0x28
0x29		Layer 4 CRC data buffer	00000000	—	R/W		Layer 4 CRC data buffer	5-38	Undefined	—	R/W	0x29
0x2A		Layer 4 CRC result display	-------0	—	R		Layer 4 CRC result display	5-39	-------0	—	R	0x2A
0x2B		Layer 4 CRC register (1/2)	00000000	—	R/W		Layer 4 CRC register (upper 8 bits)	5-39	00000000	—	R/W	0x2B
0x2C		Layer 4 CRC register (2/2)	00000000	—	R/W		Layer 4 CRC register (lower 8 bits)	5-39	00000000	—	R/W	0x2C
0x2D												
0x2E												
0x30	Analog control	Analog section control/monitor	--000000	11111110	W	Analog control	Analog test	5-40	-0000000	—	W	0x30
0x31	Power down	Power down register	-000-000	10001111	W	Power down	Power down	5-41	-000-000	—	W	0x31
0x32	Test control	Test control 0	000-----	00011111	W	Test control	Test control 0	5-42	000-----	—	W	0x32
0x33		Test control 1	-0000000	10010111	W		Test control 1	5-43	-0000100	—	W	0x33
0x34						Receive data	Receive interrupt conditions after first horizontal error correction	5-11	00100000	—	W	0x34
0x35							SI (service identifier) specification	5-12	11111111	—	W	0x35
0x37							Frame synchronization condition	5-20	-0000000	—	R/W	0x37
0x38							Receive port after second horizontal error correction	5-12	Undefined	—	R/W	0x38
0x39							Frame memory access mode	5-18	00000100	—	W	0x39
0x3B							Frame memory address (1/3)	5-19	--000000	—	R/W	0x3B
0x3C							Frame memory address (2/3)	5-19	00000000	—	R/W	0x3C
0x3D							Frame memory address (3/3)	5-19	-------0	—	R/W	0x3D
0x3E						Operating mode	Page mode/clear main channel	5-3	-0-00000	—	W	0x3E
0x0F	Extension port	Extension port	---00000	—	W	Extension port	Extension port	5-43	---00000	—	W	0x0F

MSM9563

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